ERA

WAVETEK

WAVETEK SAN DIEGO, INC.

9045 Balboa Ave., San Diego, CA 92123

INSTRUCTION MANUAL

MODEL 604
200 MHz PROGRAMMABLE
SIGNAL SWITCHER

© 1984 Wavetek

THIS DOCUMENT CONTAINS INFORMATION PRO PRIETARY TO WAVETEK AND IS SOLELY FOR INSTRU-MENT OPERATION AND MAINTENANCE. THE INFORMA-TION IN THIS DOCUMENT MAY NOT BE DUPLICATED IN ANY MANNER WITHOUT THE PRIOR APPROVAL IN WRITING FROM WAVETEK.

WAVETEK®

WAVETEK SAN DIEGO, INC.
9045 Balboa Ave., San Diego, CA 92123
P. O. Box 85265, San Diego, CA 92138
Tel 619/279-2200 TWX 910/335-2007

Manual Revision 4/84

WARRANTY

Wavetek warrants that all products of its own manufacture conform to Wavetek specifications and are free from defects in material and workmanship when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Wavetek hereunder shall expire one (1) year after delivery and is limited to repairing, or at its option, replacing without charge, any such product which in Wavetek's sole opinion proves to be defective within the scope of this Warranty. In the event Wavetek is not able to repair or replace defective products or components within a reasonable time after receipt thereof, Buyer shall be credited for their value at the original purchase price.

Wavetek must be notified in writing of the defect or nonconformity within the warranty period and the affected product returned to Wavetek's factory or to an authorized service center within thirty (30) days after discovery of such defect or nonconformity. Shipment shall not be made without prior authorization by Wavetek.

This is Wavetek's sole warranty with respect to the products delivered hereunder. No statement, representation, agreement or understanding, oral or written, made by an agent, distributor, representative or employee of Wavetek, which is not contained in this warranty, will be binding upon Wavetek, unless made in writing and executed by an authorized Wavetek employee. **Wavetek makes no other warranty of any kind whatsoever, expressed or implied, and all implied warranties of merchantability and fitness for a particular use which exceed the aforestated obligation are hereby disclaimed by Wavetek and excluded from this agreement. Under no circumstances shall Wavetek be liable to Buyer, in contract or in tort, for any special, indirect, incidental or consequential damages, expenses, losses or delays however caused.**

CONTENTS

SECTION 1 GENERAL DESCRIPTION

1.1 MODEL 604 1-1
1.2 SPECIFICATIONS 1-1
1.2 1 Switches 1-1
1.2.2 Programming 1-1
1.2.3 GPIB 1-2
1.2.4 General 1-2

SECTION 2 INSTALLATION AND INTERFACE

2.1 MECHANICAL INSTALLATION 2-1
2.2 ELECTRICAL INSTALLATION 2-1
2.2.1 Power Connection 2-1
2.2.2 Signal Connections 2-1
2.2.3 GPIB Connector 2-1
2.2.4 GPIB Address 2-1

SECTION 3 OPERATION

3.1 OPERATING THE 604 3-1
3.2 POWER UP 3-1
3.3 CONTROL PANEL OPERATION 3-1
3.3.1 Remote/Local 3-1
3.3.2 Make 1st/Break 1st 3-1
3.3.3 Multiple/Single 3-1
3.3.4 Group A Switches 3-2
3.3.5 Group B Switches 3-2
3.4 SIMPLIFIED OPERATION 3-2
3.5 REMOTE PROGRAMMING 3-4
3.5.1 Introduction 3-4
3.5.2 Data Entry 3-4
3.5.3 Executing The Program 3-5
3.5.4 Programming Switch Parameters 3-5
3.6 THE GENERAL PURPOSE INTERFACE BUS 3-5
3.6.1 GPIB Structure 3-5
3.6.2 GPIB Lines 3-6
3.6.3 Handshake Sequence 3-7
3.6.4 GPIB Commands 3-7
3.6.5 Using the GPIB 3-7
3.7 SIMPLIFIED GPIB OPERATION 3-8

SECTION 4 CIRCUIT DESCRIPTION

4.1 GENERAL DESCRIPTION 4-1
4.2 DETAILED CIRCUIT DESCRIPTION 4-1
4.2.1 Microprocessor Control 4-1
4.2.2 GPIB Interface 4-4
4.2.3 Control Panel 4-5
4.2.4 Switch Control and Switches 4-5
4.2.5 Power Supply 4-5

CONTENTS (Continued)

SECTION 5 MAINTENANCE/REPAIR

5.1 CALIBRATION 5-1
5.2 FACTORY REPAIR 5-1
5.3 BEFORE YOU START 5-1
5.4 TROUBLESHOOTING 5-1
5.5 TROUBLESHOOTING INDIVIDUAL COMPONETS 5-1
5.5.1 Digital TTL ICs 5-1
5.5.2 Three-Terminal Voltage Regulator 5-1
5.5.3 Capacitors 5-1
5.5.4 Diodes 5-1
5.6 REQUIRED TEST EQUIPMENT 5-1

SECTION 6 PARTS AND SCHEMATICS

6.1 DRAWINGS 6-1
6.2 ADDENDA 6-1
6.3 ORDERING PARTS 6-1

APPENDIX

APPENDIX A American Standard Code For Information Interchange (ASCII) A-1
APPENDIX B Program Command Summary B-1
APPENDIX C Sample Program C-1
APPENDIX D Performance Verification Setup D-1

SAFETY

This instrument is wired for earth grounding via the facility power wiring. Do not bypass earth grounding with two wire extension cords, plug adapters, etc.

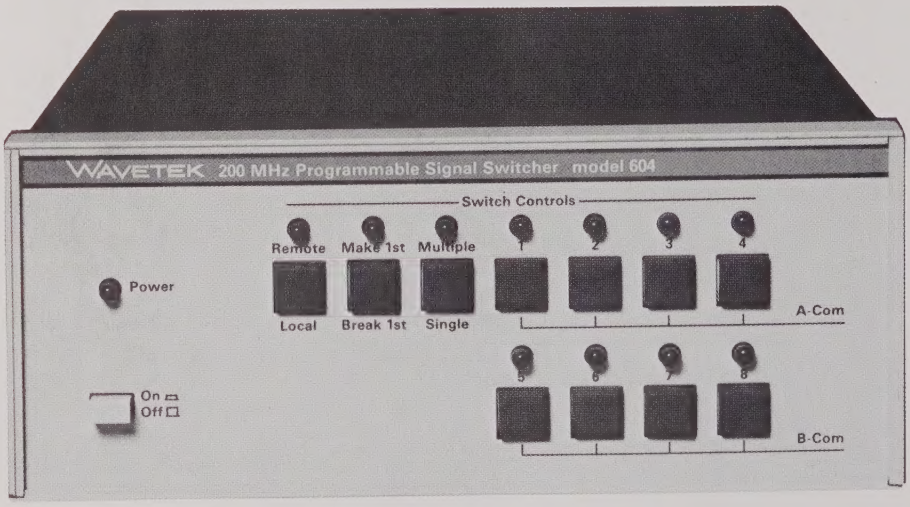
BEFORE PLUGGING IN the instrument, comply with installation instructions.

MAINTENANCE may require power on with the instrument covers removed. This should be done only by qualified personnel aware of the electrical hazards.

The instrument power receptacle is connected to the instrument safety earth terminal with a green/yellow wire. Do not alter this connection. (Reference: ⏚ or ⚠ stamped inside the rear panel near the safety earth terminal.)

WARNING notes call attention to possible injury or death hazards in subsequent operations.

CAUTION notes call attention to possible equipment damage in subsequent operations.


WAVETEK 200 MHz Programmable Signal Switcher model 604
Switch Controls
Remote
Make 1st
Multiple
1
2
3
4
Power
Local
Break 1st
Single
A-Com
On
Off
5
6
7
8
B-Com

SECTION 1
GENERAL DESCRIPTION

1.1 MODEL 604

The Model 604, a dc to 200 MHz Programmable Signal Switcher, contains two four-channel switch groups in a star configuration (see figure 1-1). Switch selection and operation along with switch modes are controlled by the front control panel or GPIB. Each switch can be opened or closed as desired. Switch modes are Make-Before-Break, Break-Before-Make, multiple channel, and single channel. Make-Before-Break mode gives maximum protection and switching flexibility while reducing the risks of saturation or overshoot in gain switching and applications involving current sources, ohmmeters,etc. Break-Before-Make mode avoids shorting two output signals such as voltage sources. Single mode allows only one of the four channels in each group to be connected to the common channel I/O. Multiple mode allows any combination of the four channels in each group to be connected to the common channel I/O.

All switch I/O BNCs are located on the rear panel. Each group of four switches share a common I/O BNC. An external connection between the two common channels allows selection of one or more of the eight available channels to the common I/O channel.

1.2 SPECIFICATIONS

1.2.1 SWITCHES

For performing verification set-up, refer to Appendix D.

Number of Switches
8 in 2 groups. See figure 1-1.

Insertion Loss
≤0.5 dB @ 100 MHz,
≤1 dB @ 200 MHz.

Crosstalk
Any channel to any channel, all switches open:
≤ – 70 dB to 10 MHz,
≤ – 50 dB to 100 MHz,
≤ – 40 dB to 200 MHz.

Isolation
One signal path, input to output, one switch open:
≤ – 55 dB to 10 MHz,
≤ – 35 dB to 100 MHz,
≤ – 30 dB to 200 MHz.

Risetime
≤2 ηs.

Maximum V/A/W
200 V, 0.5 A, 10 W.

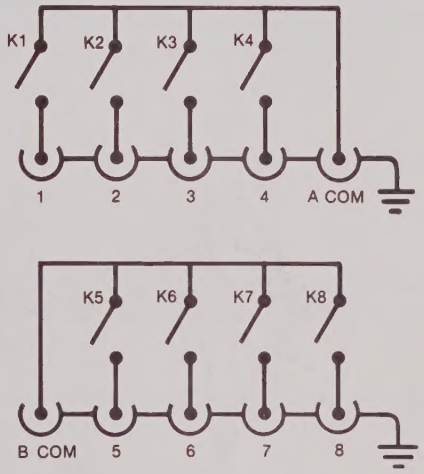


Figure 1-1. Switch Configuration

Switch Contact Resistance
≤0.25 Ω per switch.

VSWR (Typical)
≤1.03 @ 10 MHz,
≤1.15 @ 100 MHz,
≤1.51 @ 200 MHz.

Switching Time
Nominal 10 ms internal switching delay.

I/O Connections
10 BNC female connectors

1.2.2 Programming

Local and GPIB Parameters
Control of the Model 604 is via front panel controls or GPIB. Program parameters are:

Multiple/Single: Multiple allows any combination of switches to be closed. Single allows only one switch of each group to be closed.

Make 1st/Break 1st: Make 1st selects Make-Before-Break mode. Break 1st selects Break-Before-Make mode.

Open/Close: Open or close the designated switch.

Remote/Local: GPIB or front panel control selection. Remote LED lights when the 604 is under GPIB control.

GPIB Only Commands

Execute: Transfers the program to the switches. Reset: Returns the 604 to its power-on conditions.

1.2.3 GPIB

IEEE 488-1978 compatible, nonisolated, double buffered, listen only.
Address: 0-30; externally switch selectable.
Subsets: AH1, DC1, DT1, L3, RL1.
Timing: All parameters ≤25ms.

1.2.4 GENERAL

Environment

Temperature Range: 0-50°C.
Warm-up Time: 0 hours.
Altitude: Up to 10,000 ft. for operation; up to 40,000 ft. for storage.
Relative Humidity: 90% noncondensing.

Dimensions

21.6 cm (8½ in.) wide, 8.9 cm (3½ in.) high, 27.9 cm (11 in.) deep.

Weight

2.3 kg (5 lb) net; 3.6 kg (8 lb) shipping.

Mounting

Model 604 can be placed on a shelf or bench, or it can be mounted in a "half 19 inch" rack mount adapter.

Power Required

90 to 260 Vac, 48 to 66 Hz, 1 phase, ≤10 W.

SECTION 2
INSTALLATION & INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

The switcher can be used as a bench unit or rack mounted. It can be converted to rack mounts in the field.

2.2 ELECTRICAL INSTALLATION

2.1.1 Power Connection

Before rack mounting, it may be desirable to perform an initial checkout to verify operation of all functions.

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac lines supply and with a 1/8 AT fuse.

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1) according to the following procedure.

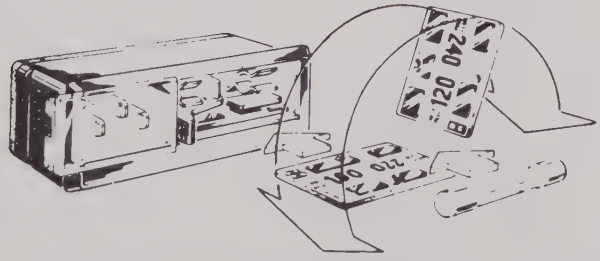


Figure 2-1. Voltage Selector and Fuse

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse-pull to left to remove the fuse.
2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.

Card Position	Input Vac	Fuse
100	90-110	1/8 AT
120	108-132	1/8 AT
220	198-242	1/16 AT
240	216-264	1/16 AT

3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.
4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

2.2.2 Signal Connections

BNC connectors, located on the rear panel, are grouped in two sets of five. Use coaxial cables equipped with BNC connectors to distribute signals to and from the switcher.

2.2.3 GPIB Connector

The GPIB I/O rear panel pin connections and signal names are given in table 2-1. The panel connector is an Amphenol 57-10240 or equivalent. GPIB interconnecting cable are available from Wavetek in 1 and 2 meter lengths.

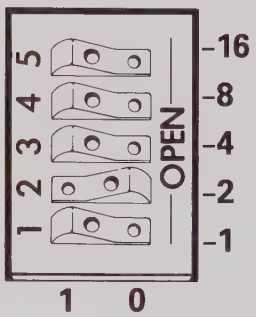
2.2.4 GPIB Address

For instrument on the General Purpose Interface Bus (GPIB), ensure that the instrument GPIB address is correct. The GPIB address can be changed by the rear panel switch (for access, see figure 2-2). The switch selections are labeled from 1 through 16 and their off position noted (off = binary "0" in table 2-2). The Model 604 only functions as a GPIB listener.

Table 2-1. GPIB Data In/Out

Pin	Signal	
1	DIO1	True When Low
2	DIO2	
3	DIO3	
4	DIO4	
5	EOI	
6	DAV	
7	NRFD	True When High
8	NDAC	
9	IFC	True When Low
10	SRQ	
11	ATN	
12		Chassis Ground ( )
13	DIO5	True When Low
14	DIO6	
15	DIO7	
16	DIO8	
17	REN	
18		Signal Gnd
19		
20		
21		
22		
23		
24		

Address Selector



NOTE: GPIB ADDRESS SELECTED IS DECIMAL 2: SWITCH 1 — OFF, 2 — ON, 3 — OFF, 4 — OFF, 5 — OFF. (TABLE 2-2: 00010).

Figure 2-2. GPIB Address Selector Switch

Table 2-2. GPIB Address Code

Device	ASCII Listen	Switch Position 16	8	4	2	1	Listen (Hexadecimal)	Device	ASCII Listen	Switch Position 16	8	4	2	1	Listen (Hexadecimal)
0	(space)	0	0	0	0	0	20	16	0	1	0	0	0	0	30
1	!	0	0	0	0	1	21	17	1	1	0	0	0	1	31
2	"	0	0	0	1	0	22	18	2	1	0	0	1	0	32
3	#	0	0	0	1	1	23	19	3	1	0	0	1	1	33
4	$	0	0	1	0	0	24	20	4	1	0	1	0	0	34
5	%	0	0	1	0	1	25	21	5	1	0	1	0	1	35
6	&	0	0	1	1	0	26	22	6	1	0	1	1	0	36
7	'	0	0	1	1	1	27	23	7	1	0	1	1	1	37
8	(	0	1	0	0	0	28	24	8	1	1	0	0	0	38
9	)	0	1	0	0	1	29	25	9	1	1	0	0	1	39
10	*	0	1	0	1	0	2A	26	:	1	1	0	1	0	3A
11	+	0	1	0	1	1	2B	27	;	1	1	0	1	1	3B
12	,	0	1	1	0	0	2C	28	<	1	1	1	0	0	3C
13	—	0	1	1	0	1	2D	29	=	1	1	1	0	1	3D
14	.	0	1	1	1	0	2E	30	>	1	1	1	1	0	3E
15	/	0	1	1	1	1	2F	31	Not allowed						

SECTION 3
OPERATION

3.1 OPERATING THE MODEL 604

Operating the Model 604 is basically selecting a switch and opening or closing the switch in the desired sequence. The Model 604 contains eight switches in two groups of four. The switches can be selected and activated by either the control panel (ref: paragraph 3.3) or a GPIB controller (ref: paragraph 3.5).

Signal connections are made using ten BNC connectors (A1-A4, A Common and B5-B10, B Common) located on the rear panel. Figure 3-1 shows the eight switches and their related BNC connectors.

Figure 3-2 shows the control panel keys and annunciators along with a reference number. Table 3-1 keys the reference number to paragraphs in this section and related paragraphs in the GPIB control section.

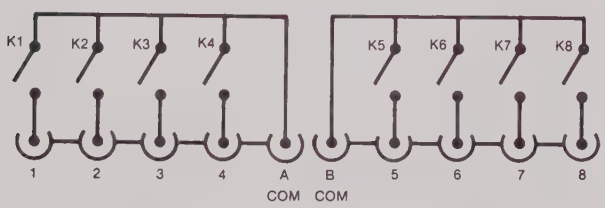


Figure 3-1. Switch Diagram

3.2 POWER UP

The power switch (1) turns the Model 604 On and Off. When power is On, the Power indicator will light. For both local and remote operation, the power must be on. All parameters at power up are set to the following conditions: Local, Break 1st, Single, and all switches open.

3.3 CONTROL PANEL OPERATION (MANUAL)

Using the control panel to select and activate the 604's switches is quite easy. Keys are divided into two groups: mode keys and switch control keys. Mode keys (Make/1st/Break 1st and Multiple/Single) select the conditions under which the switches operate. Switch control keys (1,2,3,4,5,6,7,8) immediately open or close a switch. The LED annunciator, when lit, indicate the conditions listed under it. Each key, except Power and Remote/Local, functions as toggle keys, that is, press a key once for Tone condition and a second time for the other condition.

3.3.1 Remote/Local

Pressing the Remote/Local key, 2, activates the control panel providing the 604 is not immediately receiving data over the GPIB or LLO (local lockout) is not enabled (ref: paragraph 3.6.4.1). The remote annunciator will light while receiving data over the GPIB and remains lit until the Remote/Local key is pressed, which enables the control panel.

3.3.2 Make 1st/Break 1st

The Make 1st/Break 1st key, 3, (Single mode only) selects either the make-before-break or break-before-make operation. Press the key once, if the annunciator lights, the Make 1st mode was selected; if the annunciator is out, the Break 1st mode was selected. Press the key again to select the other mode. The activation time delay selected by pressing the key is 10ms.

NOTE

Pressing the Make 1st/Break 1st key opens any closed switch in Groups A and B.

3.3.3 Multiple/Single

The Multiple/Single key, 4, selects a mode that allows either any combination of switches per group to be closed or only one switch per group to be closed. Press the key once, if the annunciator lights the Multiple mode is selected, if the annunciator is out the single mode is selected. Press the key again to select the other mode.

NOTE

Pressing the Multiple/Single key opens any closed switch in Group A and B.

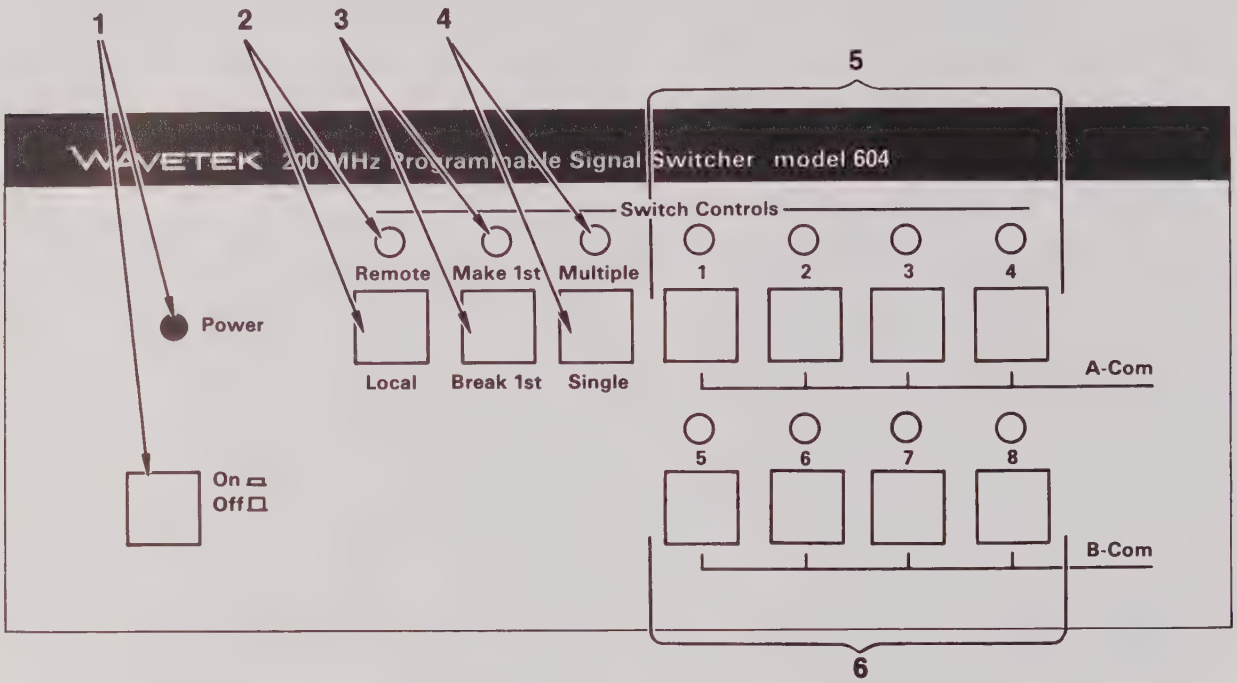


Figure 3-2. 604 Control Panel

Table 3-1. Function Cross Reference

Location In Figure	Function	Reference Paragraph
1	Power	2.2.1, 3.2
2	Remote/Local	3.3.1
3	Make 1st/Break 1st	3.3.2, 3.5.4.1, 3.5.4.2
4	Multiple/Single	3.3.3, 3.5.4.3, 3.5.4.4
5	Group A Switches	3.3.4, 3.5.4.5
6	Group B Switches	3.3.5, 3.5.4.5

3.3.4 Group A Switches

Group A consist of four switches, 5, as shown in figure 3-1, which are controlled by pressing the a key in this group. Press a key once, if the annunciator lights the switch is closed, or if the annunciator is out the switch is open. In Multiple mode the switch closes immediately, regardless of whether Make 1st/Break 1st is selected. But for single mode there will be a time delay (10 ms) before the single switch changes conditions.

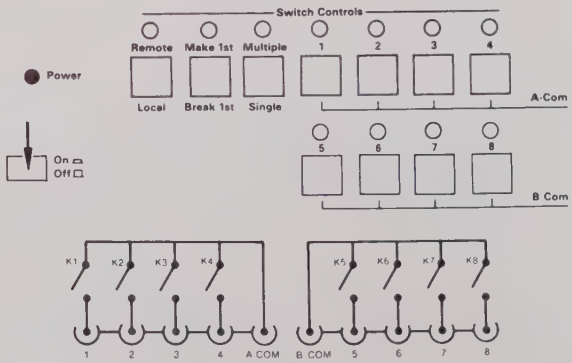
3.3.5 Group B Switches

This group of four switches, 6, functions the same as the group A switches.

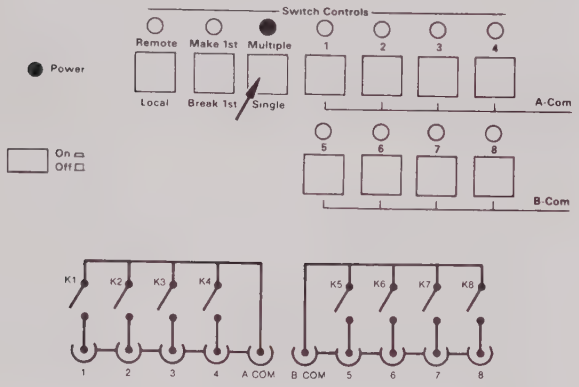
3.4 SIMPLIFIED OPERATION

The following steps provide a simplified, hands-on demonstration of the control panel keys of the 604.

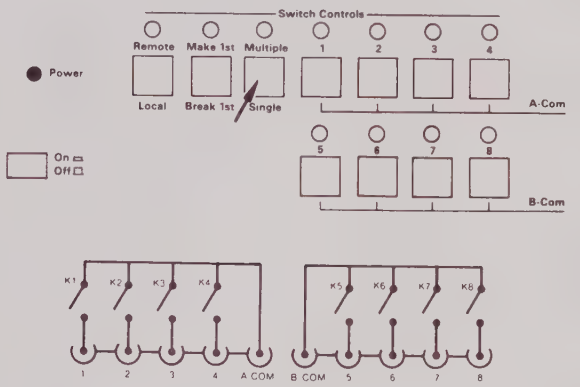
First, connect the 604 to the ac line and turn the switcher on. The 604 powers up to the Power-up (Reset) conditions: Break 1st, and Single modes with all switches open.



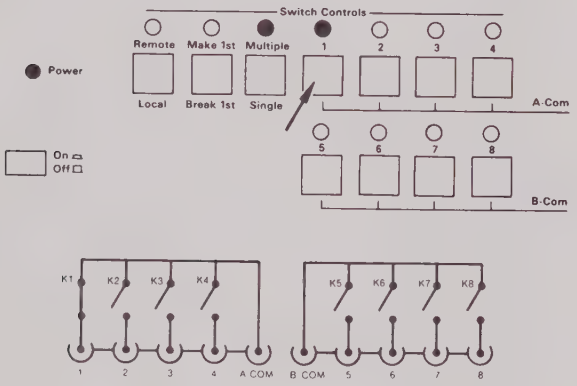
Press the Multiple/Single key once to select the multiple mode.



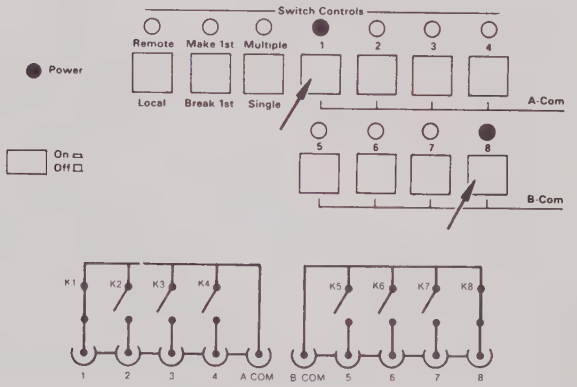
Press the **Multiple/Single** key once to select the single mode. Notice all the closed switches will open.



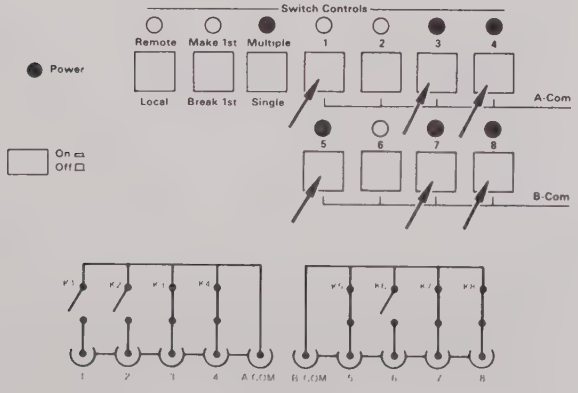
Press the key **1** to close switch 1.



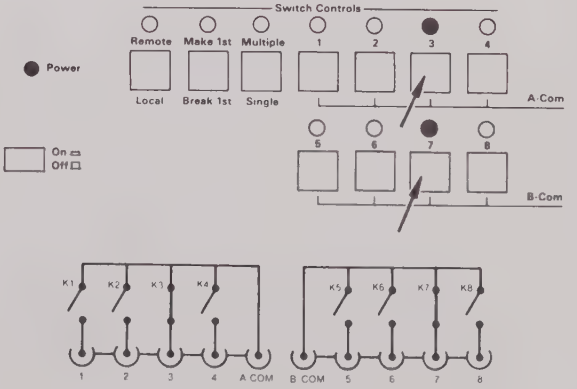
Press keys **1** and **8** once to close switches 1 and 8.



Press the key **1, 3, 4, 5, 7,** and **8** once; switch 1 opens and switches 3, 4, 5, 7, and 8 close.

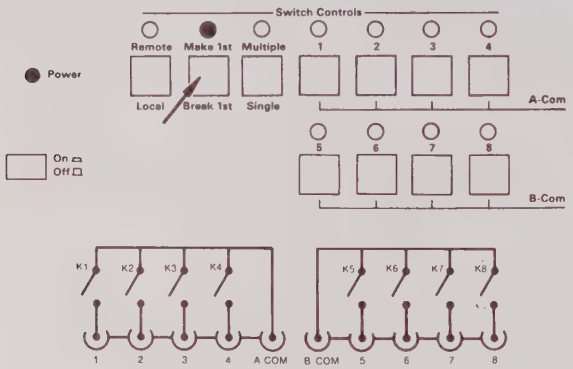


Press the keys **3** and **7** once to close swiches 3 and 7, this also opens switches 1 and 8.

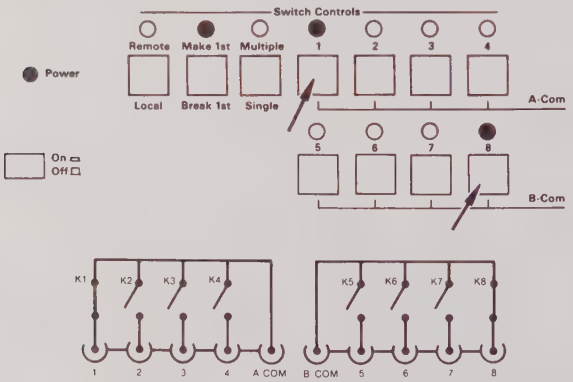


Because the 604 is in the Break 1st mode, switches 1 and 8 open, then approximately 10 ms later switches 3 and 7 close.

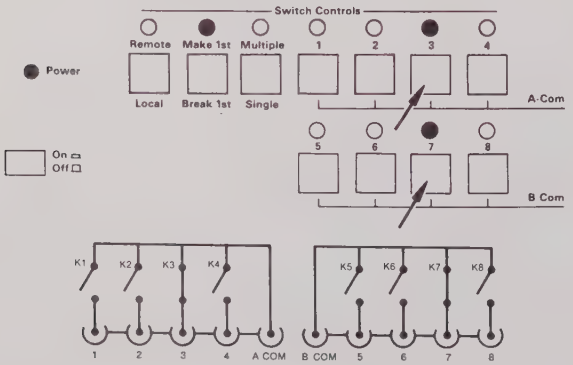
Press the **Make 1st/Break 1st** key once to select the Make 1st (Make-Before-Break) mode. Notice that all closed switches will open.



Press the keys **1** and **8** to close switches 1 and 8.



Press the keys 3 and 7 to close switches 3 and 4. Because the Make 1st mode is selected, switches 1, 8, 3, and 7 are closed for approximately 10 ms, then switches 1 and 8 open.



3.5 REMOTE PROGRAMMING (GPIB)

3.5.1 Introduction

This section describes the programming of the 604. Data may be programmed into the 604 by a GPIB controller. Paragraph 3.6 provides details concerning the GPIB. Over the GPIB all parameters, except Reset, require an execute.

3.5.2 Data Entry

The Model 604 is programmed by sending ASCII coded characters (ref: table 3-1 and Appendix B) to the microprocessor. The GPIB has priority over the control panel. Thus, if the GPIB continuously supplies data, then no data can be entered from the control panel and it appears inactive to the user. During rapid GPIB program execution, the control panel annunciators cannot be updated until the end of the program.

3.5.2.1 Characters

Characters used to program the 604 are divided into classes:

1. **Alphabetic Characters**—The upper and lower case characters A through Z select actions or commands.
2. **Numeric Characters**—The characters 1 through 8.
3. **Terminator Character**—The 604 accepts any terminator.
4. **Nonprogramming Characters**—Any character not in one of the previously described classed. They have no effect on programming and may be interspersed freely among programming characters.

Table 3-2. Model 604 Programming Codes

Command	Code	Action (A) or Parameter (P)
Multiple	T	P
Single	S	P
Close	C	P
Make First	F	P
Break First	G	P
Execute	I	A
Switch Number	K	P
Open	O	P
Reset	Z	A

3.5.2.2 Actions Vs Parameters

There are two type of commands used in the 604: parameters and actions (ref: table 3-2). There are two

types of parameters: those that do require a value and those that do not require a value; both require an execute. Actions take place immediately; they require neither a value, or execute.

3.5.2.3 Numeric Values

The digits 1 through 8 make up the numeric values. Legal values or codes depend upon the parameters selected.

3.5.2.4 Errors

Errors transmitted over the GPIB are ignored by the 604.

3.5.3 Executing the Program

A program can be executed, i.e., transferred to the switches by using an execute command (ASCII I).

GPIB **Z** command resets the 604 to the original power up conditions (ref: paragraph 3.2).

3.5.4 Programming Switch Parameters

Before programming the 604 over the GPIB verify the units is powered on (paragraph 3.2). Also, check the GPIB address (paragraph 2.2.5).

3.5.4.1 Make 1st

F causes all switches to be programmed for make-before-break operation. No numeric value is required for this parameter. The fixed delay is 10ms. This is the same a pressing the Make 1st/Break 1st key (paragraph 3.3.2) on the control panel.

3.5.4.2 Break 1st

G causes all switches in the 604 to be programmed for break-before-make operation. No numeric value is required for this parameter. The fixed delay is 10ms. This is the same as pressing the Make 1st/Break 1st key (paragraph 3.3.2) on the control panel.

3.5.4.3 Multiple

T allows any combination of switches to be closed. This parameter requires no numeric values. This is the same as pressing the Multiple/Single key (paragraph 3.3.3) on the control panel.

3.5.4.4 Single

S allows only one switch in each group to be closed. This parameter requires no numeric values. This is the same as pressing the Multiple/Single key (paragraph 3.3.3) on the control panel.

3.5.4.5 Switch Number

K followed by a numeric value selects a switch in the 604. Legal values are 1 to 8, all other values are ignored.

K1 selects switch 1
K2 selects switch 2
K3 selects switch 3
K4 selects switch 4
K5 selects switch 5
K6 selects switch 6
K7 selects switch 7
K8 selects switch 8

3.5.4.6 Open

O opens the last selected switch on receipt of an execute. No numeric values are required.

3.5.4.7 Closed

C closes the last selected switch upon receiving an execute. This parameter does not require a numeric value.

3.5.4.8 Reset

Z instantly resets the 604 to the following conditions:
All switches open.
Single mode.
Break 1st operation.

3.6 THE GENERAL PURPOSE INTERFACE BUS

This section of the manual is provided for readers who wish further background information on the GPIB.

The GPIB interface in the Model 604 is an implementation of the IEEE 488-1978 standard as a computer-to-peripheral and a peripheral-to-peripheral interface. This implementation includes all electrical, mechanical, timing and protocol considerations. It supports the following interface functions:

AH1	Complete acceptor handshake.
L3	Listen only.
RL1	Remote/local and local lockout.
DC1	Complete device clear/selective device clear.
DT1	Complete device trigger capability.

The listen capability allows a device to receive data (such as device programming information) from the bus.

3.6.1 GPIB Structure

The General Purpose Interface Bus consists of 16 negative-true signal lines as shown in Figure 3-3. These 16 lines include 8 bidirectional data lines, 3 handshake lines and 5 control lines. All devices on the bus interface to these lines with passive pull-up and active pull-down. Thus, any device may "assert" a line by pulling it down

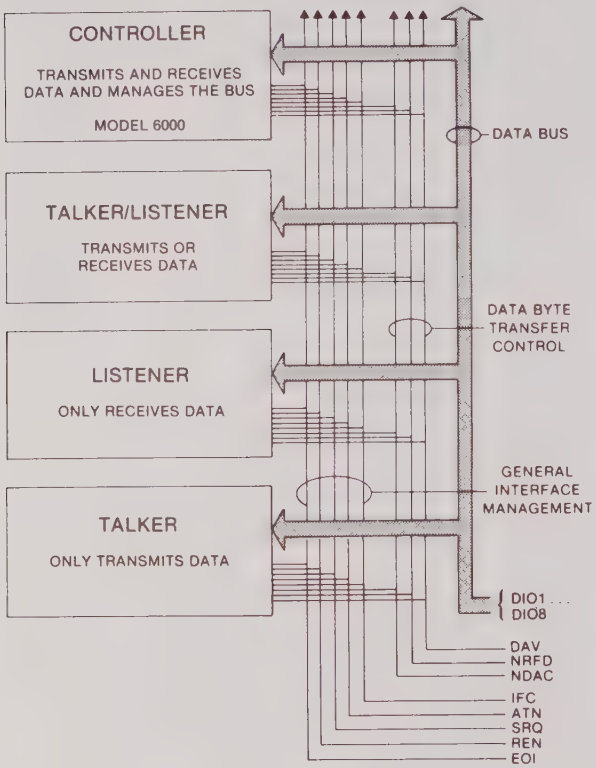


Figure 3-3. GPIB Structure

to the logic low, or "true" state. If no device is asserting the line, it is pulled up to the logic high, or "false" state. (Only the controller is allowed to assert certain lines.)

As shown in Figure 3-3, devices connected to the bus may be a LISTENER (only), TALKER (only), LISTENER/TALKER or CONTROLLER. More than one controller may be connected to the bus, but only one controller may be hard-wired as SYSTEM CONTROLLER, and only one controller at a time may assume the role of ACTIVE CONTROLLER.

3.6.2 GPIB Lines

The mnemonics used to identify the GPIB lines are:

DIO1-DIO8	Data In/Out Lines
ATN	Attention
REN	Remote Enable
DAV	Data Available
NRFD	Not Ready For Data
NDAC	Not Data Accepted
EOI	End Or Identify
SRQ	Service Request
IFC	Interface Clear

The functions of the GPIB lines are:

DIO1-DIO8 These eight lines (Data In/Out) are used to send commands from the controller and to transfer data back and forth between instruments and the controller.

ATN The Attention line is operated only by the active controller. It specifies whether the information on lines DIO1-DIO8 is data (ATN false) or a command (ATN true). Whenever ATN is set true, no activity is allowed on the bus except for controller-originated messages.

REN The Remote Enable line controls whether devices on the GPIB are in local or remote modes. In the local mode, devices respond to front panel commands and do not respond to GPIB originated commands. In remote mode, the situation is reversed; GPIB originated commands are obeyed, while front panel commands are ignored. The Wavetek 604 enters the remote state when it receives its listen address and REN is enabled. The Wavetek 604 then stays in the remote mode until the REN line is put in the local state, a Go To Local (GTL) command is received or the LCL front panel key is pressed.

DAV, NRFD, NDAC These are the "handshake" lines (Data Valid, Not Ready For Data and Not Data Accepted) which regulate the transmission of information over the lines DIO1-DIO8. For each command or data byte transferred, a complete handshake cycle occurs. This handshake is designed to hold up the bus until the slowest device has accepted the information. A description of the handshake cycle is given in the next paragraph, after the definition of the GPIB lines.

EOI When ATN is false, EOI (End Or Identify) indicates that the data on lines DIO1-DIO8 is the last byte of a data message. When the Wavetek 604 receives a data byte with EOI true, it automatically supplies a terminator character following the data byte. When the Wavetek 604 transmits the last byte of a message (which is always a terminator character) it also sets EOI S true.

IFC — The Interface Clear line is asserted by the system controller to reset the interface logic in all devices connected to the bus to a known initial state.

3.6.3 Handshake Sequence

The three handshake lines, Data Valid (DAV), Not Ready for Data (NRFD) and Not Data Accepted (NDAC) are used in a typical data exchange as follows:

All devices currently designated as active listeners would indicate (via the NRFD line) when they are ready for data. A device not ready would pull this line low (ground), while a device that is ready would let the line float high. Since a low overrides a passive high, this line will stay low until all active listeners are ready for data. When the talker senses this, it places the next data byte on the data lines and then pulls DAV low. This tells the listeners that the information on the data lines is valid and that they may read it. Each listener (at its own speed) then takes the data and lets the NDAC line go high. Again, only when all listeners have let NDAC go high will the talker sense that all listeners have read the data. It can then remove DAV (let it go high) and start the entire sequence over again for the next byte of data.

3.6.4 GPIB Commands

Commands are sent over lines DIO1-DIO8 to the 604 Swith ATN true are divided into three classes:

1. Listen Address
2. Universal Commands

   DCL Device Clear
   LLO Local Lockout
3. Addressed Commands
   GTL Go To Local

These commands and command groups are shown with their binary codes in Appendix A.

3.6.4.1 Listen Addresses

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 20 through 3E, ASCII codes SP through >). A 32nd address, called unlisten (hexadecimal 3F, ASCII ?) is used to command all devices to not read data bytes. The Wavetek 604 listen address is selected by rear panel switches (Figure 2-2) which specifies the lower 5 bits of the address (ref: table 2-2).

3.6.4.2 Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the Wavetek 604 are:

1. Device Clear (DCL) — Resets the Wavetek 604 to the initial power-on settings. DCL affects all devices on the bus.
2. Local Lockout (LLO) — Causes the Wavetek 604 to enter a state where the front panel LCL key is inoperative. In this state, the keyboard is disabled and the instrument will only accept parameter changes through the GPIB. To enable keyboard control, the GPIB controller must place the REN line in the local state.

3.6.4.3 Addressed Commands

Addressed commands are used to command a device to perform designated actions. The instruments recognizes the addressed commands when addressed as a listener. Go To Local (GTL) — Commands the Wavetek 604 to go to the local mode.

3.6.5 Using the GPIB

This GPIB section of this manual has deliberately been placed after the REMOTE OPERATION section, because in actual practice the GPIB is much easier to use than its description would indicate. Some points to remember when programming GPIB controller:

1. It is not necessary to use separate listen or talk addresses, or to worry about the ASCII or hexadecimal equivalent of the address. Simply program the decimal device number, which is same number previously programmed into the Wavetek 604 with the rear panel address switches.
2. When using the standard WRITE command, it is not necessary to program the state of the ATN line, etc. The controller performs these "handshake" functions automatically. (Some controllers have an alternate command, such as COMMAND @, that will allow the advanced programmer access to individual commands such as "attention" and "unlisten".)
3. The GPIB mnemonics (DCL, GET, etc.) are not necessarily the actual commands used by the controller. For example, on the controller used to write the sample programs in this manual, the command with the GPIB mnemonic GET translates to an actual controller command of TRG @.
4. Controller GPIB commands are not part of the standardized BASIC computer language, and the commands will vary from one make of controller to the next. Refer to the GPIB programming manual for your make of controller.

3.7 SIMPLIFIED GPIB OPERATION

This section gives example statements using a GPIB controller to select and activate remotely the 604's switches. In these examples a Wavetek Model 6000 Instrument Controller was used. If another controller is used consult its user/operators manual for the proper statements. The string in quotation marks will always be the same regardless of the controller. Also, Appendix C contains a demonstration routine for the 604.

For this example, set the 604's GPIB address switch (ref: paragraph 2.2.5) to 11. If a different address is used, make the appropriate changes to the WRITE @ statements. First, connect the 604 to the controller. Next, connect the 604 to the ac source and turn the 604 on. Remember, the 604 powers up in the Break 1st and Single modes with all switches open.

A typical statement used to control the 604 might be WRITE @711:"K1CI".

Where:

WRITE @—The BASIC statement for the Model 6000 controller, may vary with different controllers.

711—GPIB address 11.

"K1CI"—The 604 command string. Notice that over the bus an execute command I is required.

A simple explanation follows each statements. Some examples use two statements, these examples are grouped together and setup the following conditions.

WRITE @711:"TI"
Selects the multiple mode. This opens any closed switches if the 604 was in the single mode.

WRITE @711:"SI"
Selects the single mode. This opens any closed switches if the 604 was in the multiple mode.

WRITE @711:"FI"
Selects the make 1st mode. This opens any closed switches if the 604 was in the break 1st mode.

WRITE @711:"GI"
Selects the break 1st mode. This opens any closed switches if the 604 was in the make 1st mode.

WRITE @711:"SFI"
Selects the single and make 1st modes. This opens any closed switches if the 604 as in the multiple or break 1st modes.

WRITE @711:"SGI"
Selects the single and break 1st modes. This opens any closed switches if the 604 was in the multiple or make 1st modes.

WRITE @711:"SGK1CK5CI"
Selects the single and break 1st modes, and closes switches 1 and 5, all closed switches are automatically opened.

WRITE @711:"TK1CK3CK5CK8CI"
Selects the multiple mode and closes switches 1, 3, 5, and 8.

WRITE @711:"TK1CK5CI"
WRITE @711:"K10K2CK8CI"
The first statement selects the multiple mode and closes switches 1 and 5. The second statement opens switch 1 and closes switches 2 an 8; switch 5 remains closed.

WRITE @711:"SGK1CK5CI"
WRITE @711:"K2CK8CI"
The first statement selects the single and break 1st modes, and closes switches 1 and 5. The second statement opens switches 1 and 5, waits the standard 10ms, and closes switches 2 and 8.

WRITE @711:"SFK1CK5CI"
WRITE @711:"K2CK8CI"
The first statement selects the single and make 1st modes, and closes switches 1 and 5. The second statement closes switches 2 and 8 (switches 1, 2, 5, and 8 will all be closed), waits the standard 10ms, and opens switches 1 and 5.

SECTION 4
CIRCUIT DESCRIPTION

4.1 GENERAL DESCRIPTION

The Model 604, 200 MHz Programmable Signal Switcher, consists of five major blocks (see figure 4-1): microprocessor control, GPIB interface, control panel, switch control and switches, and power supply. Each of these blocks are described briefly in this general description and in greater detail in paragraph 4.2.

Microprocessor Control. The microprocessor is the clearinghouse for all control operations. Through its program in Read-Only-Memory (ROM), the microprocessor accepts commands from the IEEE-488 GPIB or control panel, then translates them into internal operating parameters and sends them to the switch circuits. The microprocessor also stores these parameters in Random-Access-Memory (RAM) and displays them on the control panel annunciators.

GPIB Interface. The GPIB interface provides a means to interface between the IEEE 488-1978 bus and the microprocessor control section within the 604. The 604 functions only as a listener, thus it can only receive commands over the bus.

Control Panel. The control panel allows manual control of the 604's switches. The panel consists of sets of keys and annunciators. All power, input data, and output data for the panel are provided, via an interconnecting cable, from the GPIB/Microprocessor board.

Switch Control and Switches. This section receives control data from the microprocessor control block and uses that data to energize or de-energize the proper relay. Eight relays make up the dual four channel switches.

Power Supply. The 604 contains a single +5V power supply which supplies all the power to the 604's circuits.

4.2 DETAILED CIRCUIT DESCRIPTION

4.2.1 Microprocessor Control

The microprocessor control section (figure 4-2) is located on the GPIB/Microprocessor circuit board, accessible beneath the top cover of the 604. Descriptions in this section include the microprocessor/memory, reset monitor, and software.

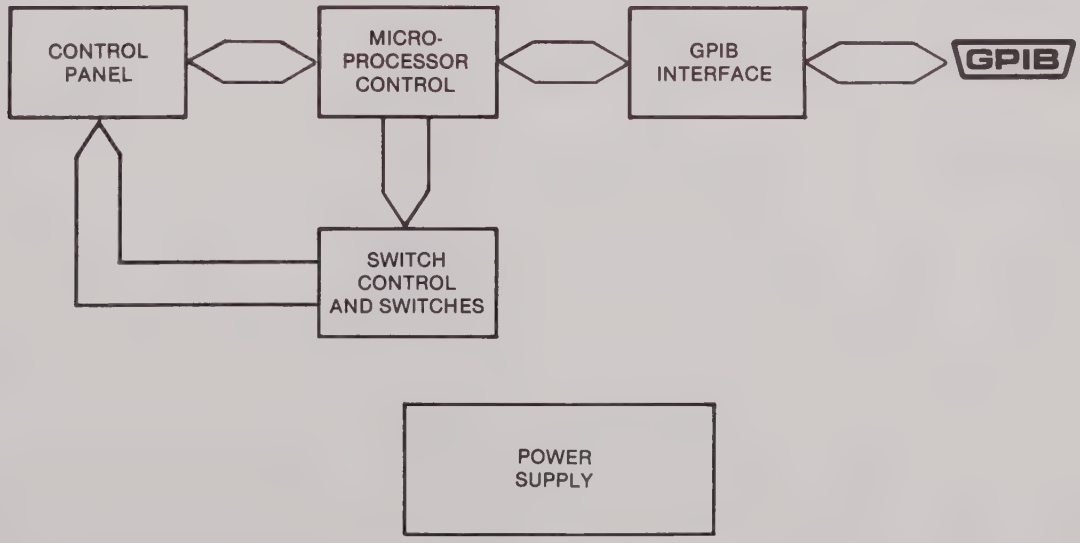


Figure 4-1. 604 Block Diagram

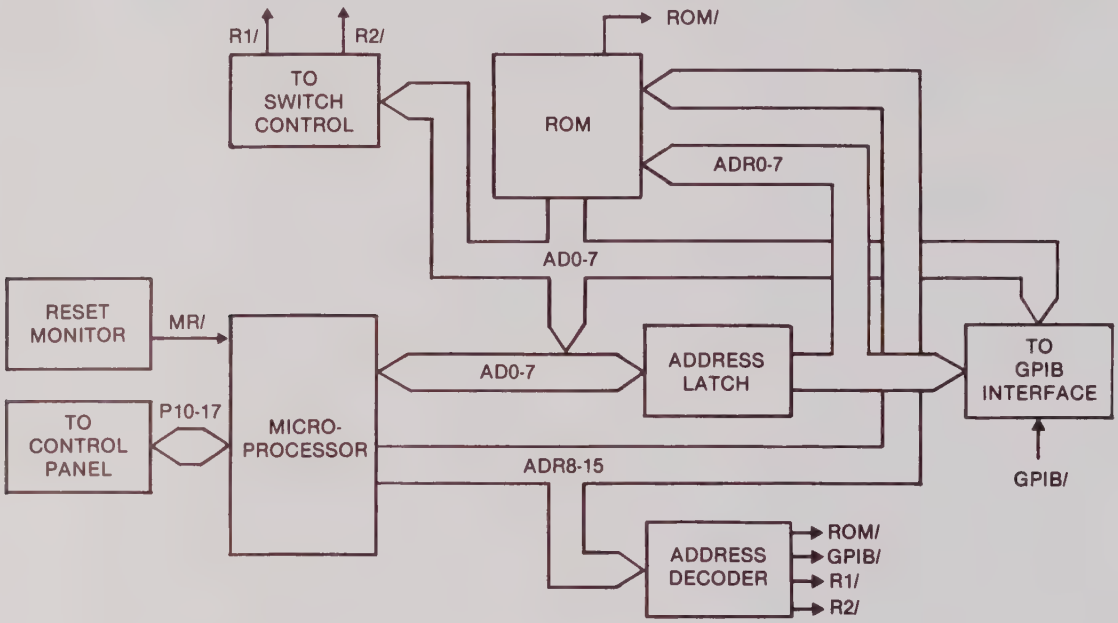


Figure 4-2. Microprocessor Control

4.2.1.1 Microprocessor/Memory

The microprocessor/memory section includes the microprocessor itself, an address latch to demultiplex the lower-order address bits, an address decoder to select appropriate memory locations and addressable registers, and Read-Only-Memory (ROM).

Table 4-1. Memory Map

Addressable Devices	Address (Hex)
Microprocessor Internal Reg	0000-001F
N/A	0020-007F
Internal RAM	0080-00FF
N/A	0100-01FF
External Test Program	2000-3FFF
R1-Group A Register	4000-4FFF
R2-Group B Register	5000-5FFF
N/A	6000-7FFF
GPIB	8000-BFFF
N/A	C000-D7FF
ROM	D800-DFFF
N/A	E000-FFDF
Vector	FFE0-FFFF

Microprocessor. The 6803 microprocessor, U3, operates in its expanded-multiplexed mode (mode 2), as determined by mode control pins 8, 9, and 10. This mode allows the microprocessor to address external memory by using port 3 (P30-P37) as the lower-order address/data bus, port 4 (P40-P47) as the high-order address bus with pins 39 and 48 as the address strobe (AS) and read/write line (R/$\overline{W}$) respectively. Ports 1 (P10-P17) and 2 (P20-P24) are always I/O ports.

A clock-generating circuit within the microprocessor uses an external 4 MHz crystal, Y1, between the XTAL 1 and XTAL 2 (pins 2 and 3) to develop its internal phase clock and the 1 MHz system enable clock (E). Figure 4-3 shows the approximate timing for major signals and busses in the microprocessor/memory system. Actual system timing varies somewhat from instrument to instrument, so signal spacing may be different within the 1μs period of the system clock.

The microprocessor responds to three interrupt inputs: master reset (MR/), which initializes the microprocessor; the external interrupt request line (IRQ/), which the GPIB interface uses to signal the processor; and the non-maskable interrupt (NMI/), which is not used in the 604, available only at the test connector.

Address Latch. An octal latch, U4, demultiplexes the address/data bus from the microprocessor to hold the lower-order addresses (ADR0-ADR7) during the part of the E clock cycle that data occurs. The address is latched on the negative transition of the AS signal (U3 pin 39). See timing diagram, figure 4-3.

Address Decoder. A dual 1 of 4 decoder, U7, decodes the four highest address lines (ADR12-ADR15) to enable one of four possible addressable devices. These are the IEEE-488 interface (GPIB/), Read-Only-Memory (ROM/), and each of the relay/display interface registers (R1/ and R2/).

ROM. A 2k × 8 Read-Only-Memory (ROM), U5, contains the program for the microprocessor. The ROM/ line from address decoding, U7, enables U5, whose output is enabled on the rising edge of the E clock.

RAM. The microprocessor, U3, uses its own internal Random-Access-Memory (RAM) as a scratch pad memory.

4.2.1.2 Reset Circuit

The reset circuit, a power reset monitor, ensures proper system reset at power up or down. It also reacts to power line faults by generating a master reset (MR/) and, thereby, inhibiting memory access and opening all switches.

The reset circuit consists of two voltage comparators, U2A and B. Any sudden changes in power supply voltage greater than 500mV sets the comparator output low, thus generating a master reset (MR/) for the microprocessor.

4.2.1.3 Software

Although a detailed description of software is beyond the scope of this manual, some discussion of the microprocessor operation is helpful in understanding how the instrument functions.

Figure 4-4 shows the two main program loops for microprocessor operation: background and parser-procedure loops. The background loop only checks registers for interrupt flags set by external or timer interrupts. The parser selects and calls procedures when the program enters it, and returns control to the background loop when a procedure is finished.

Background Loop. The background loop inspects the two internal registers (GPIB, keyboard) for interrupt flags (nonzero status) and then returns to its beginning. If no

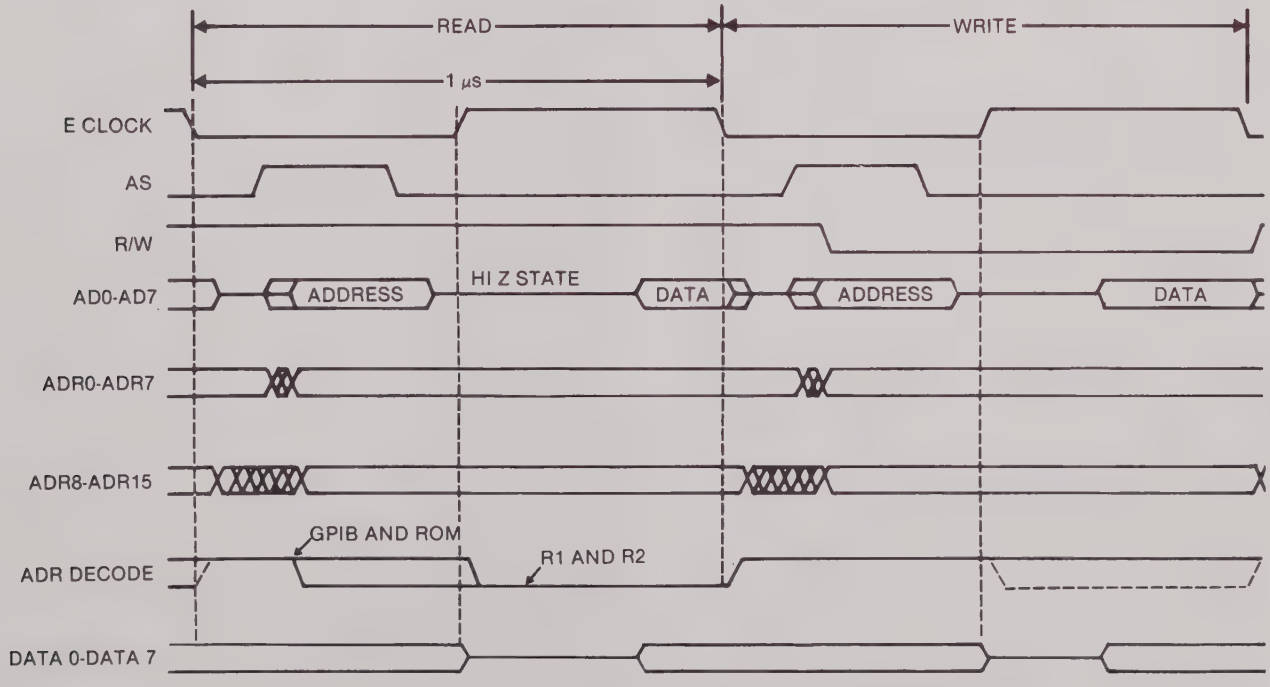


Figure 4-3. Microprocessor Timing Diagram

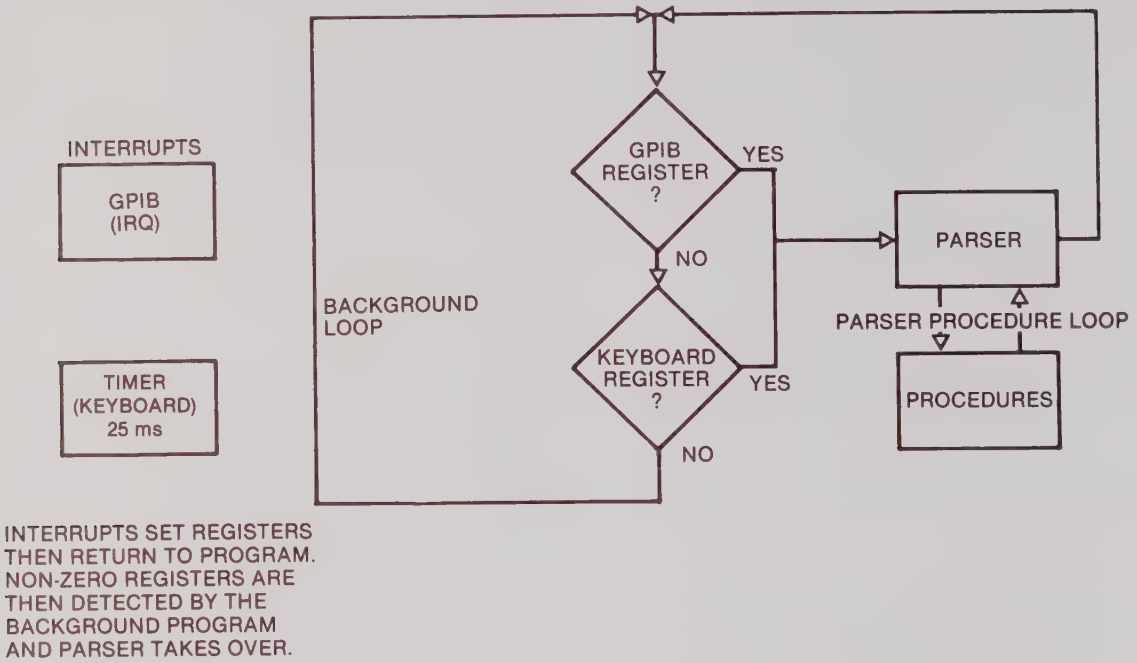


Figure 4-4. Program Loop

interrupt flags are set the entire loop takes about 50 to 60μs. If a flag is set, the loop time increases by the length of the interrupt procedure. If either of the first two registers flags are set, the background program calls the parser.

Parser/Procedure. The parser handles all programming chores except short housekeeping routines. When the parser is called, it examines a series of registers and decides which routines are required, then calls the required procedure which, when complete, returns control to the parser. When the parser has scanned all inputs, it returns control to the background loop. Even if their functions appear simple, the parser and the procedures with their interpretive functions make up the bulk of the program.

Interrupts. There are two ways the processor program can be interrupted: through IRQ/ (generated by the GPIB interface) or through an internal timer (used for all other interrupt requirements).

GPIB Interrupts — GPIB interrupts are initiated by the GPIB responding to GPIB bus commands. When the interrupt occurs, a byte is read from the GPIB interface and stored in a register. The program then returns to its preinterrupt position. It is the background program that actually inspects the register and passes control to the parser, which in turn decides what routine is called to process the information.

Timer Interrupts — Keyboard scans are run during initial power-up and every 25ms during the time the instrument is on. These subroutines are initiated when the number in the clock register (within the microprocessor) matches the preset number in the timer register (within the microprocessor). Upon completion of the subroutine, the preset number corresponding to the elapsed time required between successive interrupt for the function is again added to that interrupt register. The clock timer continues to increment its own register, and when the number in this register again matches the interrupt register, the subroutine is initiated. These interrupt registers work independently of each other and may set another register (as in the keyboard interrupt) or they may initiate and entire subroutine.

4.2.2 GPIB Interface

4.2.2.1 GPIB Adapter

The GPIB adapter interfaces with the instrument's microprocessor and handles all the handshake protocol and data transfer over the IEEE-488 General Purpose Interface Bus (GPIB). See GPIB/Microprocessor schematic (0103-00-1224 sheet 2).

The IEEE 488 interface IC, U8, does all the handshaking requirements of the 1978 IEEE-488 standard. When the controller on the bus sends the instrument's listen address, U8 signals the instrument's microprocessor by asserting the interrupt request line, IRQ/ (a low on U8 pin 40). The processor can then interrogate any of the eight registers internal to U8. Data from the IEEE-488 bus (listen mode) is accessed by reading from the data register in U8. The address strobe enable line (ASE/) from the interface IC, U8, controls the select line to U12 that enables the GPIB address switch, SW2. The microprocessor can read this switch by a read of the address register in U8 which causes U8 to set ASE/ low during the E clock (data) portion of the microprocessor clock cycle. The address is stored in U8 by writing into the internal address register.

4.2.2.2 GPIB Switch Buffer

A five section DIP switch (SW2) selects the GPIB address for the instrument. IEEE-488 specifications alow only 31 possible addresses for GPIB instruments (binary 0-30).

The address switch buffer consists of five switches, SW2, and an octal buffer, U12; the buffer is enabled by the ASE/ line from the GPIB interface.

4.2.3 Control Panel

The control panel, a separate printed circuit board, allows manual control of the 604. It contains 11 keys and 12 light emitting diode (LED) annunciators. See the front panel schematic (0103-00-1225) in the rear of this manual.

The keys connect through a cable directly to the microprocessor, U3, ports 10, P11, P12, P13, P15, P16, and P17, which functions as the key scanning circuit. Periodically the microprocessor polls the keys to determine if a key was pressed and exactly which key was pressed.

The LED displays connects through the cable from the two Relay/Display drivers, which are located on the GPIB/Microprocessor board. These drivers receive their inputs from the microprocessor data bus.

4.2.4 Switch Control and Switches

The switch control and switch section consists of the relay/display driver, U10 and U11, and relays K1-K8. The relay/display drivers receives parallel data directly from the microprocessor control section. Each of the 8 outputs, RA1/-RA4/ and RB1/-RB4/, from U10 and U11 drives each relay. In addition, the relay/display drivers control the annunciator on the control panel.

4.2.5 Power Supply

The circuits in the Model 604 are powered by a single + 5V supply, located on the GPIB/Microprocessor board. The supply consists of a single three-terminal regulator (VR1) that normally operates with a 1.25V difference between its output and reference terminals.

In the + 5V supply (GPIB/Microprocessor schematic), ac from the transformer, T1, is rectified by CR1 and filtered by C1 to provide unregulated dc for the regulator, VR1. A resistive divider, R17 and R18, sets the voltage at the reference input, pin 1, to provide an output of + 5V at E2, while C22 and C23 provide additional filtering at the output of the regulator. CR11 prevents C23 from discharging back through the regulator when power to the instrument is turned off.

SECTION 5
MAINTENANCE/REPAIR

5.1 CALIBRATION

The Model 604 Signal Switcher requires no calibration. For performance verification set-up refer to Appendix D. If, for any reason, this unit fails to function correctly, refer to paragraph 5.4, Troubleshooting, or return the unit to Wavetek for repair.

5.2 FACTORY REPAIR

Wavetek maintains a Customer Service department. If an instrument is returned to Wavetek for repair, a detailed description of the specific problem should be attached to the unit to minimize turnaround time.

5.3 BEFORE YOU START

Since no troubleshooting guide can possibly cover all potential problems, the aim of this guide is to give a methodology which, if applied consistently, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description in conjunction with the schematic. Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

5.4 TROUBLESHOOTING

Table 5-1 gives an index of common symptoms. For each symptom a troubleshooting step is referenced that will aid in the solution of the problem. Individual component troubleshooting is given in paragraph 5.5, recommended test equipment is given in paragraph 5.6, and circuit schematics are in the back of this manual.
In all problems:

1. Double check for proper parameter settings.
2. Verify power supplies ar in specification.
3. Inspect components, wiring and circuit boards for heat damage.

Find the instrument symptom in table 5-1 and proceed as directed to the proper troubleshooting step. After verifying the referenced step is okay, proceed to the following step unless directed otherwise.

5.5 TROUBLESHOOTING INDIVIDUAL COMPONENTS

5.5.1 Digital TTL IC's (e.g. 7400 series)

1. The correct operating voltage for the output high state is $>+2.4$V and low state is $<+0.5$V.

Table 5-1. Symptoms

Symptoms	Step in Table 5-2
Display does not light	1.1-1.3
Display incorrect at power up	2.1-2.2
Keyboard has no effect	3.1-3.2
Will not work on GPIB	4
Cannot correctly control switches	5

2. The input must show the same two levels as in step 1. If the levels are between $+0.8$V and $+2$V, the connection to the driving circuit output is open.

5.5.2 Three-Terminal Voltage Regulator

1. To operate correctly, the control pin must be 1.25V less than the output pin.
2. Also, the input pin must be at least 2V greater than the output pin.

5.5.3 Capacitor

1. Shorted capacitors have 0V across their terminals.
2. Open capacitors usually can be located by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.

5.5.4 Diodes

A signal diode is defective if there is a greater than 1V (typically 0.7V) forward bias across it. Light emitting diodes (LED) operate with a 1.2 to 2V forward bias.

5.6 REQUIRED TEST EQUIPMENT

Oscilloscope . . . . . Bandwidth >10 MHz.
Digital Voltmeter . . . . . Ohms and dc volts.

Table 5-2. Troubleshooting

Step	Symptom	Check	Reference Paragraph	Major Components	Schematic (No./Sheet/ Location)
1.1	Display does not light.	AC Power		—	—
		a. Power Source	2.2.1	—	1267/1/C7
		b. Power Cord	2.2.1	—	1267/1/C7
		c. Power Fuse	2.2.1	—	1267/1/C7
		d. Power Section	2.2.1	—	1267/1/C7
		e. Power Switch	—	—	1224/2/D8
1.2		DC Power +5V supply	4.2.5	T1, CR1, C1, C3, C8, R1, R2, CR2, VR1	1224/2/D4
1.3		Control Panel Interconnect Cable	—	W1, J14, J15, P15	0253/1/C6, 1225/1/D2, 1224/2/B3
2.1	Display incorrect at power up.	Microprocessor			
		a. Reset Circuit	4.2.1.2	U2	1224/2/C7
		b. E-clock	4.2.1.1	U3	1224/1/D7
		c. Address Strobe (AS)	4.2.1.1	U3, U4	1224/1/D6, D7
		d. Address/Data Bus (AD)	4.2.1.1	U3, U4, U8, U5, U10, U11, U12	1224/1,2
		e. Address Bus (ADR)	4.2.1.1	U3, U4, U6, U7, U5	1224/1
2.2		Control Panel			
		a. Display Driver	4.2.3	U10, U11	1224/2/B6, C6
		b. Display	4.2.3	CR1-CR11	1225/1/A4-C4
		c. Connector Cable	—	W1, J14, J15, P15	0253/1/C6, 1225/1/D1, 1224/2/B3
3.1	Keyboard has no effect.	Microprocessor Board	4.2.1.1	U3	1224/1/D7
3.2		Control Panel	4.2.3	SW1-SW11	1225/1/C3-C7
4	Won't work on GPIB.	GPIB			
		a. Address Switch	4.2.2.2, 2.2.4	SW2, U12	1224/2/A8, A7
		b. Interface	4.2.2.1	U8	1224/1/D5
5	Cannot correctly control switches.	Relay/Display Drivers	4.2.4	U10, U11	1224/2/C6
		Relays	4.2.4	K1-K8	1224/2/B2-D2

APPENDIX A
AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII)

b7 b6 b5 / BITS / b4 b3 b2 b1 / column row	0_0	MSG[1]	0_1	MSG	$0_1{}_0$	MSG	$0_1{}_1$	MSG	$1_0{}_0$	MSG	$1_0{}_1$	MSG	$1_1{}_0$	MSG	$1_1{}_1$	MSG
	0		1		2		3		4		5		6		7	
0 0 0 0 / 0	NUL		DLE		SP	MLA ASSIGNED TO DEVICE	0	MLA ASSIGNED TO DEVICE	@	MTA ASSIGNED TO DEVICE	P	MTA ASSIGNED TO DEVICE	\	MEANING DEFINED BY PCG CODE	p	MEANING DEFINED BY PCG CODE
0 0 0 1 / 1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0 0 1 0 / 2	STX		DC2		"		2		B		R		b		r	
0 0 1 1 / 3	ETX		DC3		#		3		C		S		c		s	
0 1 0 0 / 4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0 1 0 1 / 5	ENQ	PPC[3]	NAK	PPU	%		5		E		U		e		u	
0 1 1 0 / 6	ACK		SYN		&		6		F		V		f		v	
0 1 1 1 / 7	BEL		ETB		'		7		G		W		g		w	
1 0 0 0 / 8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1 0 0 1 / 9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1 0 1 0 / 10	LF		SUB		*		:		J		Z		j		z	
1 0 1 1 / 11	VT		ESC		+		;		K		[		k		{	
1 1 0 0 / 12	FF		FS				<		L		\		l		|	
1 1 0 1 / 13	CR		GS		-		=		M		]		m		}	
1 1 1 0 / 14	SO		RS		.		>		N		^		n		~	
1 1 1 1 / 15	SI		US		/		?	UNL	O		_	UNT	o		DEL	

ADDRESSED COMMAND GROUP (ACG)

UNIVERSAL COMMAND GROUP (UCG)

[4] LISTEN ADDRESS GROUP (LAG)

TALK ADDRESS GROUP (TAG)

PRIMARY COMMAND GROUP (PCG)

SECONDARY COMMAND GROUP (SCG)

[1]MSG = INTERFACE MESSAGE
[2]b1 = DIO1 . . . b7 = DIO7
[3]REQUIRES SECONDARY COMMAND
[4]DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	=	DCL	Device clear	Universal Command Group
DC1	=	LLO	Local lockout	
NAK	=	PPU	Parallel poll unconfigure	
EM	=	SPD	Serial poll disable	
CAN	=	SPE	Serial poll enable	
SOH	=	GTL	Go to local	Addressed Command Group
EOT	=	SDC	Selected device clear	
ENQ	=	PPC	Parallel poll configure	
BS	=	GET	Group execute trigger	
HT	=	TCT	Take control	

APPENDIX B
PROGRAMMING COMMAND SUMMARY
(Excluding GPIB Command Groups Given in Appendix A)

Control and Data Name	Control Panel Key	ASCI Character
1, 2, 3, . . ., 8	1, 2, 3, . . ., 8	1, 2, 3, . . ., 8
Multiple	Multiple/Single	T
Single	Multiple/Single	S
Close	—	C
Make 1st	Make 1st/Break 1st	F
Break 1st	Make 1st/Break 1st	G
Execute	—	I
Switch	—	K
Open	—	O
Reset	—	Z

APPENDIX C
SAMPLE PROGRAM

The following program, written in BASIC, demonstrates how a GPIB controller, in this example a Wavetek Model 6000 Instrumentation Controller, controls a Model 604 signal switcher. The 604's address, in this example, is set to 11. If a different address is used, make the appropriate changes in the "WRITE @" commands. Because BASIC commands may vary, depending upon the controller, changes may need to be made in the program; pay particular attention to the commands that send data to the 604, such as WRITE @ in program line 120. Also, the WAIT DELAY statements (lines 151, 210, 271, and 281) can be altered to speed up or slow down the routine.

SAMPLE PROGRAM

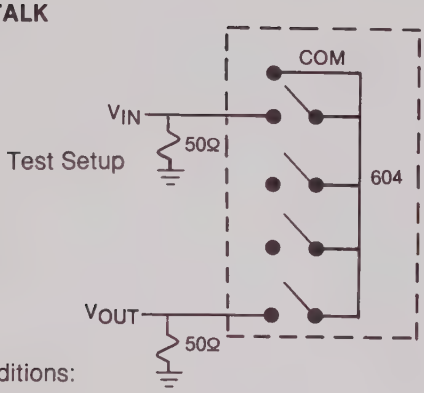
```
100 CLEAR
110 PRINT "Model 604 sample program"
120 WRITE @711:"Z"
130 FOR A=1 TO 10
140 FOR B=1 TO 8
150 WRITE @711:"SK";B;"CI"
160 WAIT DELAY .5
170 NEXT B
180 WRITE @711:"Z"
190 NEXT A
200 FOR A=1 TO 10
210 FOR B=1 TO 8
220 WRITE @711:"FTK";B;"CI"
230 WAIT DELAY .1
240 NEXT B
250 WRITE @711:"SI"
260 NEXT A
270 FOR A=1 TO 20
280 WRITE @711:"FTK1CK2CK3CK4CI"
290 WRITE @711:"K5CK6CK7CK8CI"
300 WAIT DELAY .15
310 WAIT @711:"SFI"
320 WAIT DELAY .15
330 NEXT A
340 GOTO 120
350 END
```

Sample Program Explanation

100	Clear the controller.
120	Resets the 604 to the power up/reset conditions.
130-190	Selects the single mode, closes and opens each switch in sequence, and resets. Repeats this cycle 9 times.
200-260	Selects the multiple and make 1st modes, then closes each switch. Next selects the single mode which opens all switches at once. Repeats this cycle 9 times.
270-330	Selects the multiple and make 1st modes, closes all the switches in group A at once, then closes all the switches in group B at once. Then selects the single mode which opens all switches at once. Repeats this cycle 19 times.
340	Returns the program to line 120.

APPENDIX D
PERFORMANCE VERIFICATION SETUP

CROSSTALK

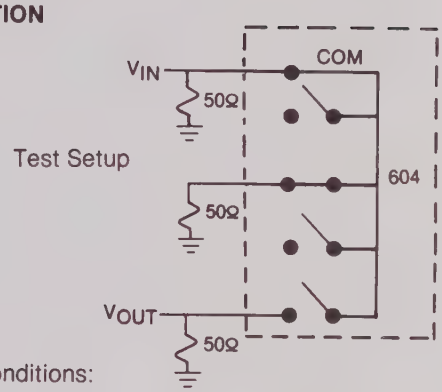


Test Conditions:

All switches open.
Input and output terminated with 50Ω.
Measured from any channel to any other channel.

$$\text{Crosstalk (dB)} = 20 \text{ Log } \frac{\text{Vout}}{\text{Vin}}$$

ISOLATION

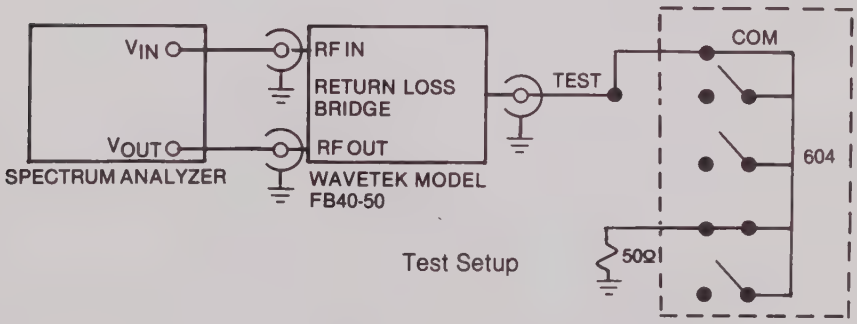


Test Conditions:

Test switch open; one switch closed and terminated.
Signal input to COM (A or B).
Input and output terminated with 50Ω.

$$\text{Isolation (dB)} = 20 \text{ Log } \frac{\text{Vout}}{\text{Vin}}$$

VSWR



Test Conditions:

Close switch on measured channel, other switches open.
Terminate measured channel with 50Ω.

Test Procedure

1. Disconnect cable at TEST.
   Measure Baseline (V_1) in dB on Spectrum Analyzer.
2. Connect cable at TEST. With switch closed and terminated (50Ω) take second reading (V_2) in dB on Spectrum Analyzer.
3. Calculate Return Loss.
   Return Loss (dB) = (V_1)—(V_2).

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	ASSY DRWG, REAR PANEL
3	JACK SCREW
1	REAR PANEL
P1 P2	CONN, HOUSING
J1	RECEPTACLE
9	SOLDER LUG
8	PIN, MALE
7	PIN, FEMALE
F1	FUSE, 1/8A, 250V, S
12	GROMMET, RUBBER
6	SCREW, HEX NUT, CA PLATE 6-32
4	NUT, PRESS, FLOATING (6-32)
10	WASHER, FLAT, #6 BIN 495
5	WASHER, SPLIT LOCK 6
11	SLEEVING, BLACK #4

WAVETEK PARTS LIST	TITLE ASSY, REAR PANEL MODEL 604

REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	WIRE, HU, 20GA, GRN/Y
NONE	WIRE, HU, 22GA
NONE	WIRE, HU, 22GA
NONE	WIRE, HU, 22GA
NONE	WIRE, HU, 22GA
NONE	WIRE, HU, 22GA
NONE	WIRE, HU, 22GA
NONE	WIRE, HU, 22GA
NONE	WIRE, HU, 22GA
2	ASSY, RIBBON CABLE 24/26 PIN

WAVETEK PARTS LIST	TITLE ASSY, REAR PANEL MODEL 604

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS-ACCUPRESS REORDER NO A27086

REV	ECN	BY	DATE	APP

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
0102-00-1267	WVTK	0102-00-1267	1
1400-01-0530	WVTK	1400-01-0530	2
1400-01-7820	WVTK	1400-01-7820	1
03-09-1093	MOLEX	2100-02-0106	2
6VJ1	CORCM	2100-03-0026	1
11A144	ZIER	2100-04-0025	1
02-09-2118	MOLEX	2100-05-0005	2
02-09-1118	MOLEX	2100-05-0026	6
MDL 1/8	BUSMN	2400-05-0001	1
2188	ACCUR	2800-10-0007	1
MS35649-264	COML	2800-14-6100	2
AS-632-1	PEM	2800-16-0015	4
#6FLAT WASHER	CMRCL	2800-26-6001	2
#6SRLW	CMRCL	2800-42-6000	2
SLEEVING, BLACK #4	NATBR	3000-00-0025	1

	ASSEMBLY NO. 1101-00-1267 PAGE: 1	REV

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
HH0-317, UL1430	JUDD	6000-32-0045	1
15U-BLACK	GAVTT	6000-32-2000	1
15U-BROWN	GAVTT	6000-32-2001	1
15U-RED	GAVTT	6000-32-2002	1
15U-BLUE	GAVTT	6000-32-2006	1
15U-GRAY	GAVTT	6000-32-2008	1
15U-WHITE	GAVTT	6000-32-2009	1
15U-WHITE/BLACK	GAVTT	6000-32-2090	1
15U-WHITE/GRAY	GAVTT	6000-32-2098	1
6002-00-0028	WVTK	6002-00-0028	1

	ASSEMBLY NO. 1101-00-1267 PAGE: 2	REV

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST REAR PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ·010 ANGLES ·1 XX ·030		
	DO NOT SCALE DWG		MODEL NO 604 / DWG NO 1101-00-1267 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, FRONT PANEL	0101-00-1225	WVTK	0101-00-1225	1
NONE	SCHEMATIC, FRONT PANEL	0103-00-1225	WVTK	0103-00-1225	1
NONE	FRONT PANEL PCB	1700-00-1225	WVTK	1700-00-1225	1
R1 R10 R11 R12 R2 R3 R4 R5 R6 R7 R8 R9	RES, CAR, 1/8W, 5%, 20	RCR05-200JS	AB	4700-05-2009	12
RN1 RN2	RES MODULE, 470	4116R-001-471	BOURN	4770-00-0036	2
CR1 CR10 CR11 CR12 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9	LED	TIL-220	TI	4899-00-0006	12
SW1 SW10 SW11 SW2 SW3 SW4 SW5 SW6 SW7 SW8 SW9	SWITCH, DISC, SPST	MDPA005	SHADW	5199-00-0006	11
W1	ASSY, RIBBON CABLE 24/26 PIN	6002-00-0027	WVTK	6002-00-0027	1

WAVETEK PARTS LIST	TITLE PCA, FRONT PANEL MODEL 604	ASSEMBLY NO. 1100-00-1225 PAGE: 1	REV

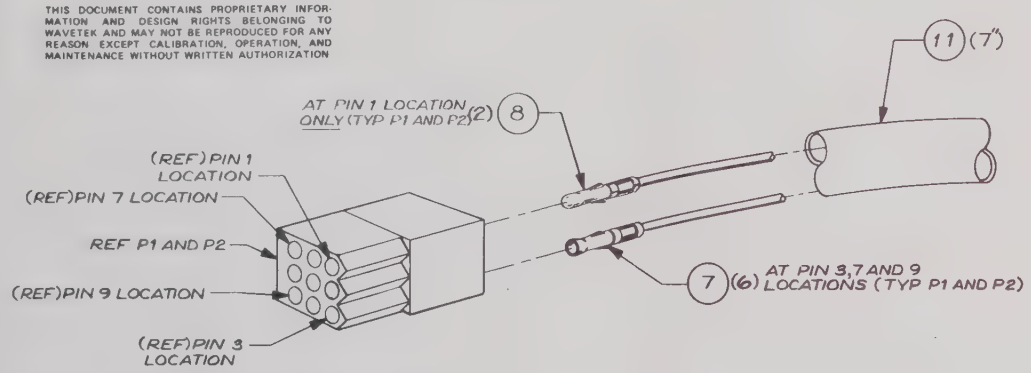
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PARTS LIST FRONT PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO 604 / DWG NO 1100-00-1225 / REV
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 1
	SCALE		

BISHOP GRAPHICS ACCUPRESS REORDER NO A27000

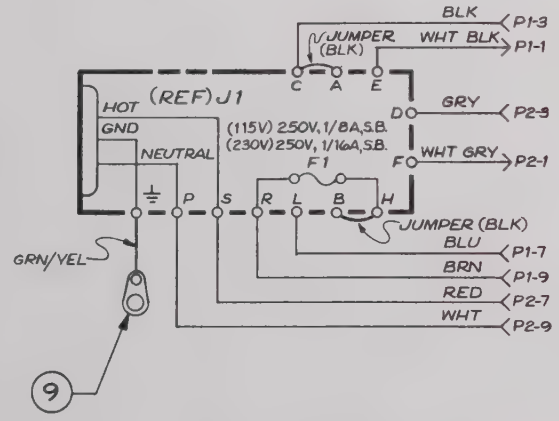
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

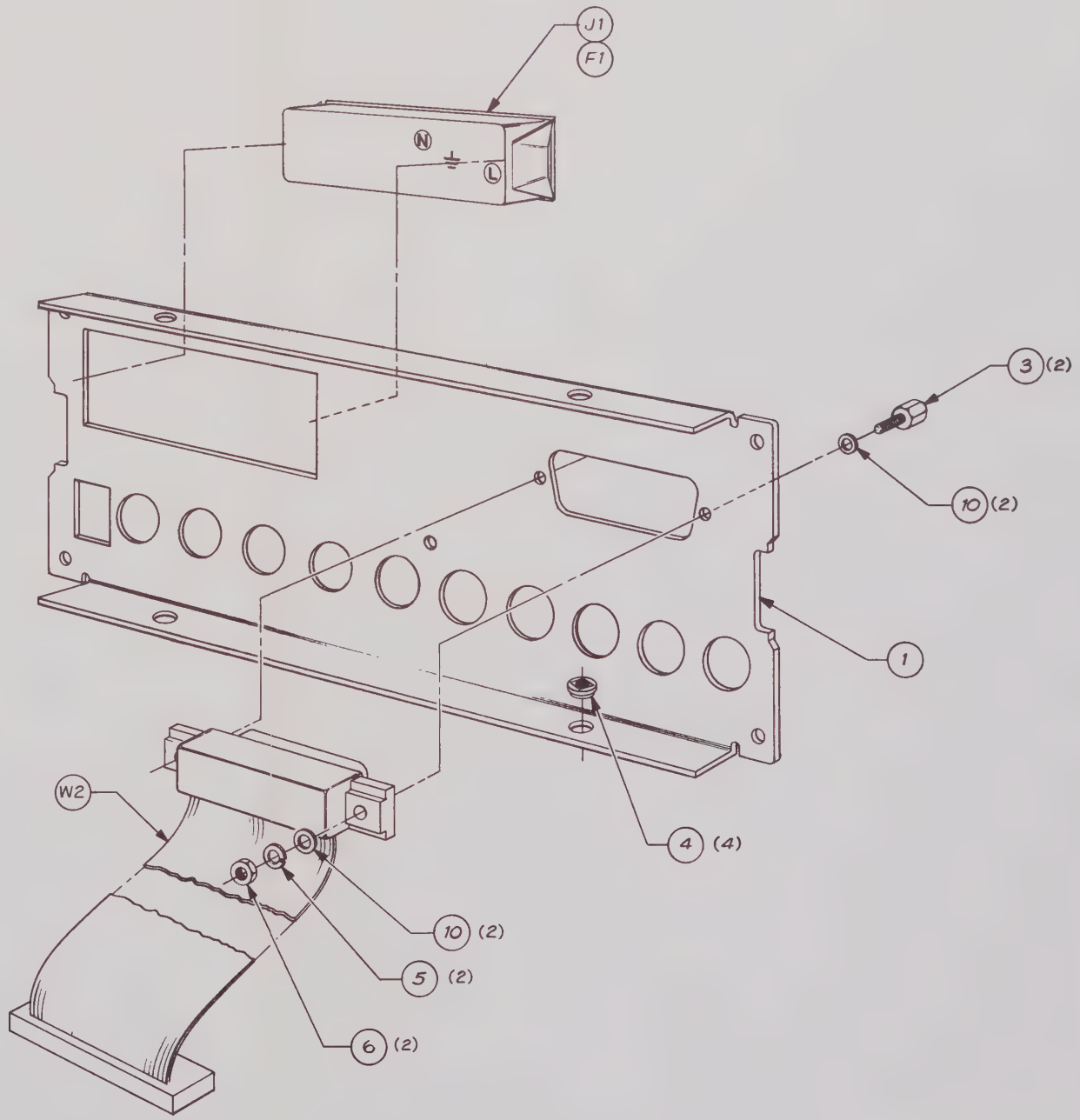
REV	ECN	BY	DATE	APP

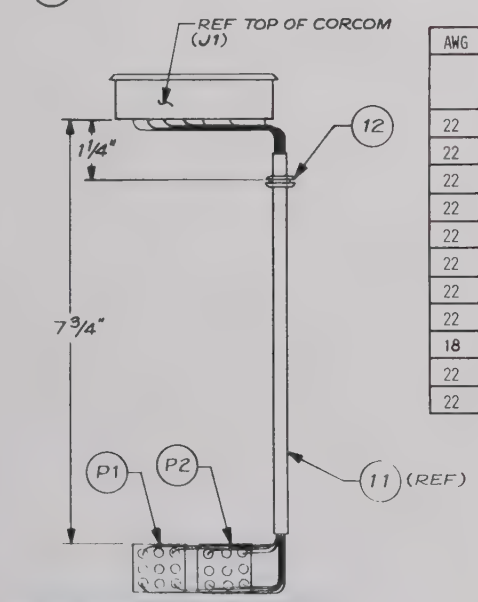

11 (7")
AT PIN 1 LOCATION ONLY (TYP P1 AND P2) (2)
8
(REF) PIN 1 LOCATION
(REF) PIN 7 LOCATION
REF P1 AND P2
(REF) PIN 9 LOCATION
(REF) PIN 3 LOCATION
7 (6) AT PIN 3,7 AND 9 LOCATIONS (TYP P1 AND P2)

DETAIL "A"

CONNECTOR CONFIGURATION
TYP FOR P1 AND P2







WIRING HARNESS CONFIGURATION

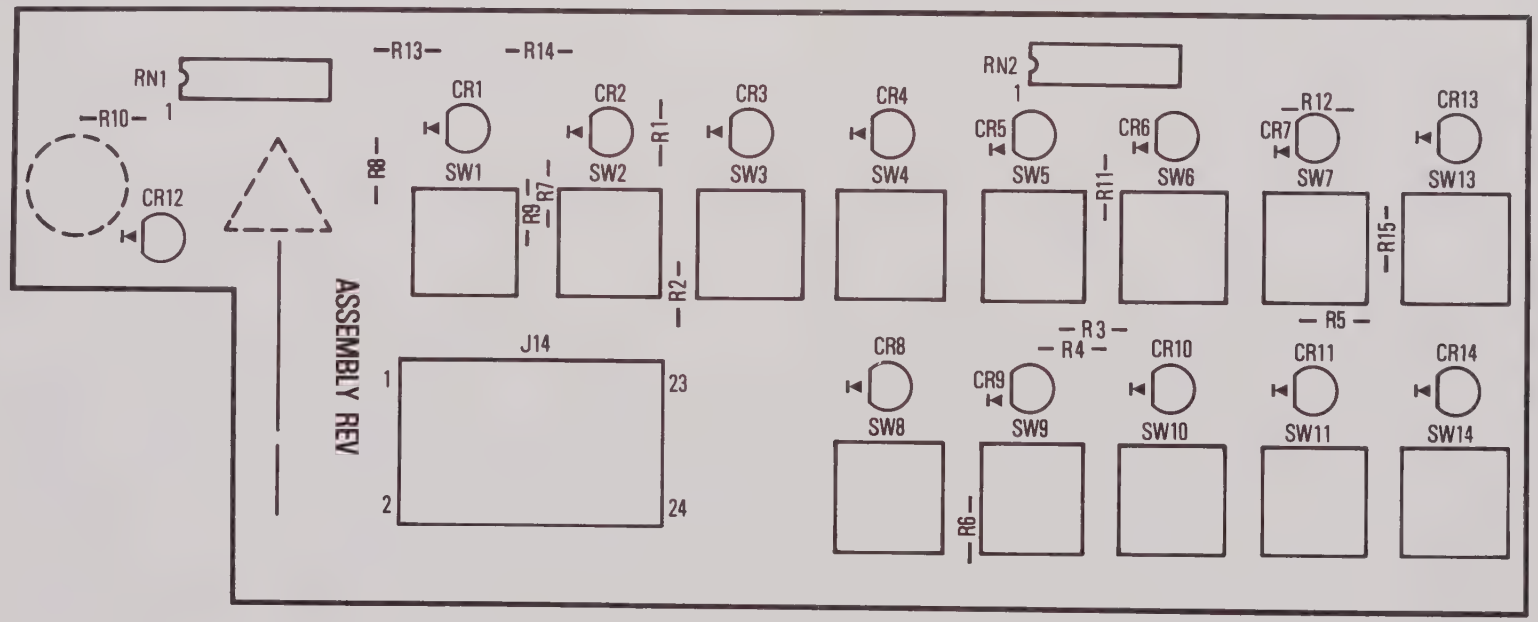
REAR PANEL WIRE LIST

AWG	COLOR	LENGTH	DESTINATION		
			FROM "CORCOM" (J1)	TO	
22	WHT/BLK	10"	J1-E	P1-1	W4
22	BLK	11"	J1-C	P1-3	
22	BLU	10"	J1-L	P1-7	
22	BRN	10"	J1-R	P1-9	
22	WHT/GRY	10 1/2"	J1-F	P2-1	
22	GRY	11 1/2"	J1-D	P2-3	
22	RED	10"	J1-S	P2-7	
22	WHT	11"	J1-P	P2-9	
18	GRN/YEL	4"	J1-⏚	ITEM 9	
22	BLK	1/2"	J1-H	J1-B	
22	BLK	1/2"	J1-A	J1-C	

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 3/2/84	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY, REAR PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO 604
	SCALE NONE		DWG NO 0102-00-1267 REV
			CODE IDENT 23338 SHEET 1 OF 1

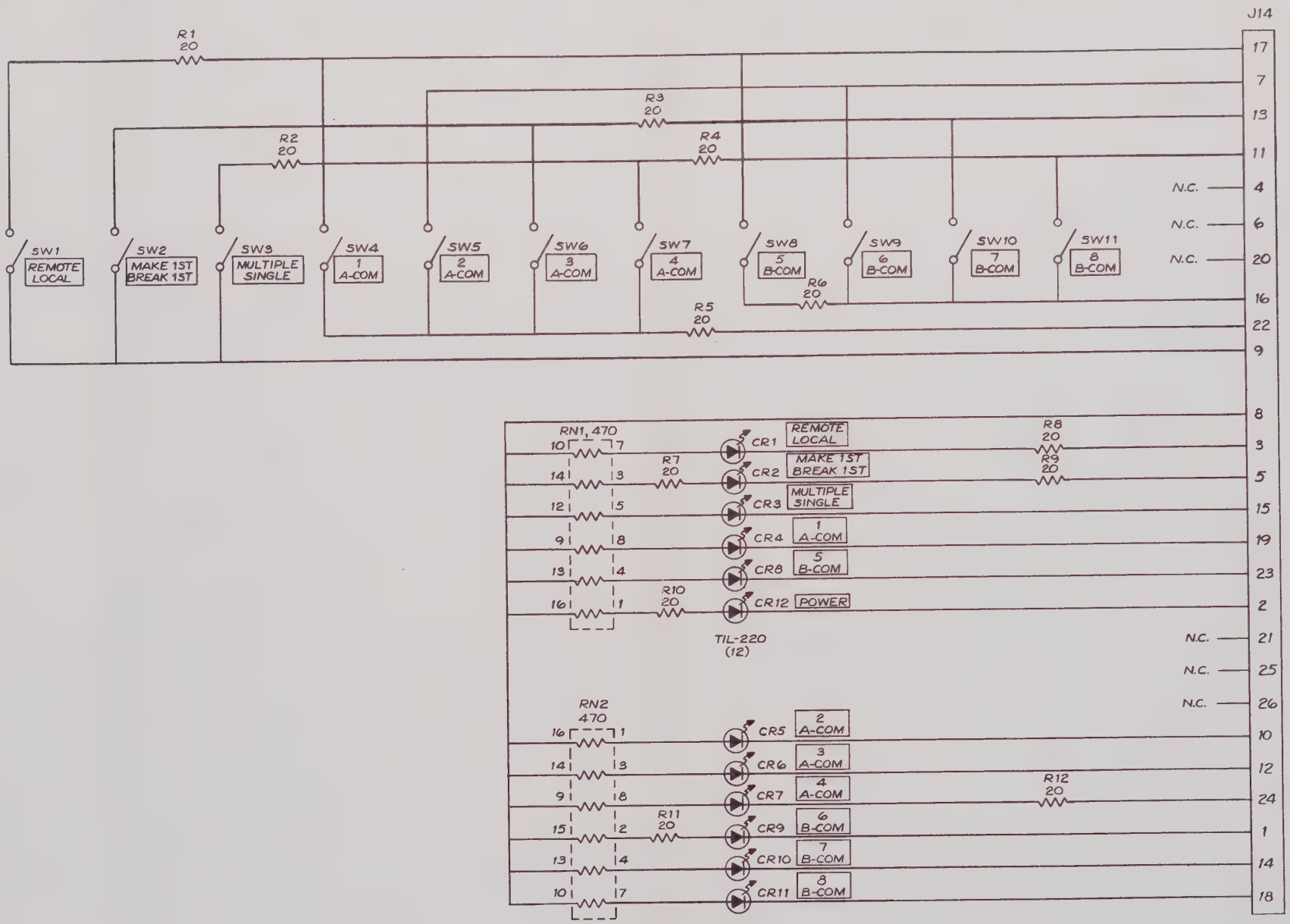
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: FRONT PANEL ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		
	DO NOT SCALE DWG	MODEL NO	DWG NO 1100-00-1225 REV
	SCALE	CODE IDENT 23338	SHEET OF

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP



1. ALL RESISTORS ARE 1/8W, 5%, CARBON, IN OHMS.

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 3/4/84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC, FRONT PANEL BOARD
	RELEASE APPROV	4/24/84	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 604	DWG NO 010-00-1225 REV
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

POWER SUPPLY

CHASSIS, P18, J18, VR1 LM317, CR1 3N254, CR2 IN4002, T1, J1, J2, SW1, POWER, C1 3300/50V, C3 100/25V, C8 .1/50V, R1 165, R2 499, +5V REG, TP3, TP4, TP5, J17 CAMBION JUMPER E1 E2, +5V

CHANNEL A 4 CHANNEL SWITCH

RA1/, RA2/, RA3/, RA4/, C22–C25 .1/50V, K1–K4, C30 .1/50V, J4–J7, J8 A COM, C31 .1/50V, RV2 RV1 E3, J9 B COM, C32 .1/50V, RB1/, RB2/, RB3/, RB4/, C26–C29 .1/50V, K5–K8, J10–J13, C33 .1/50V, +5V

CHANNEL B 4 CHANNEL SWITCH

TEST CONNECTOR J16

(1D7) E → 1
(1C6) ADR15 → 2
→ 3
(1C6) ADR14 → 4
(1D6) AS → 5
(1C6) ADR13 → 6
→ 7
(1C6) ADR12 → 8
(1D8) NMI/ → 9
(1C6) ADR11 → 10
→ 11
(1C6) ADR10 → 12
→ 13
(1C6) ADR9 → 14
→ 15
(1C6) ADR8 → 16
→ 17
(1D6) AD7 → 18
→ 19
(1D6) AD6 → 20
→ 21
(1D6) AD5 → 22
(1B8) TEST/ → 23
(1D6) AD4 → 24
→ 25
(1D6) AD3 → 26
+5V → 27
(1D6) AD2 → 28
(C7) MR/ → 29
(1D6) AD1 → 30
N.C. → 31
(1D6) AD0 → 32
→ 33
(1D7) R/W → 34

RESET CIRCUIT

+5V, C9 .1/50V, R3 1K, R5 100K, R4 100K, R6 51.1, R7 10K, C11 .1/50V, R21 1M, R8 51.1, C2 10/25V, R19 100K, R9 100K, R10 1K, U2-D, U2-C, U2-A, U2-B, 1/4 LM399, MR/ (1C5),(1D8) (B1), N.C.

RELAY/DISPLAY DRIVERS

C19 .1/50V +5V, U10 74LS 374, C20 .1/50V +5V, U11 74LS 374, (1D6) AD0–AD7, (1C8) P24, (1A5) R1/, R2/, RA1/–RA5/, MBB/, MULT/, REM/, RB1/–RB5/, ABC/, N.C.

J15
RB2/ → 1
→ 2
REM/ → 3
RB5/ → 4
MBB/ → 5
RA5/ → 6
(1C8) P11 → 7
+5V → 8
(1C8) P15 → 9
RA2/ → 10
(1C8) P13 → 11
RA3/ → 12
(1C8) P12 → 13
RB3/ → 14
MULT/ → 15
(1C8) P17 → 16
(1C8) P10 → 17
RB4/ → 18
RA1/ → 19
(1C8) P14 → 20
ABC/ → 21
(1C8) P16 → 22
RB1/ → 23
RA4/ → 24
N.C. → 25
N.C. → 26

ADDRESS SWITCH BUFFER

RN3 10K, +5V, ADDRESS SELECTOR, SW2, C21 .1/50V, U12 74LS 244, (1D6) AD0–AD7, ASE/ (1D5)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 9/1/84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR	4/24/84	TITLE: SCHEMATIC, GPIB/MICROPROC BD.
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 604	DWG NO 0103-00-1224 REV
	SCALE	CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, MICROPROC BD MODEL 604	0101-00-1224	WVTK	0101-00-1224	1
NONE	SCHEMATIC, MICROPROC MODEL 604	0103-00-1224	WVTK	0103-00-1224	1
10	LABEL, CAUTION	1400-01-1400	WVTK	1400-01-1400	1
12	SHIELD, POWER	1400-01-7723	WVTK	1400-01-7723	1
19	COVER, PWR SWITCH REF 3200-03-0019	1400-01-7961	WVTK	1400-01-7961	1
C4 C5	CAP, CER, MN, .01MF, 50V	CAC02Z5U103Z100A	CORNG	1500-01-0310	2
C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C8 C9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	25
C6 C7	CAP, MICA, 27PF, 500V	DM15-270J	ARCO	1500-12-7000	2
C2	CAP, ELECT, 10MF/25V RADIAL LEAD, SP .10	CRE SERIES 10/25	CAPAR	1500-31-0002	1
C3	CAP, ELECT, 100MF, 25V RADIAL LEAD, SP .20	CRE SERIES 100/25	CAPAR	1500-31-0102	1
C1	CAP, ELECT, 3300MF, 50V RADIAL LEAD, SP .40	CRE SERIES 3300/50	CAPAR	1500-33-3202	1
14	DBL COATED FOAM TAPE	4262 1/2" X 216FT	3M	1600-02-0010	1
13	MICROPROC PCB	1700-00-1224	WVTK	1700-00-1224	1

WAVETEK PARTS LIST | TITLE: PCA, MICROPROC BD MODEL 604 | ASSEMBLY NO. 1100-00-1224 | PAGE: 1 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	MODEL 604				
J10 J11 J12 J13 J4 J5 J6 J7 J8 J9	CONNECTOR, BNC(PC)	227161-1	AMP	2100-01-0019	10
J18	CONN HEADER 3 PIN	640456-3	AMP	2100-02-0116	1
P18	HEADER, CONN 3 PIN	640440-3	AMP	2100-02-0117	1
J15 J3	CONN, HEADER 26 PIN/2 ROW	929836-01-13	A/P	2100-02-0156	2
J1 J2	PC MOUNT CONNECTOR 9 PIN	09-18-5094	MOLEX	2100-02-0157	2
2	SKT, IC, 24PIN	DILB-24P-108	BURND	2100-03-0029	1
1	SKT, IC, 40PIN	DILB-40P-108	BURND	2100-03-0030	2
3	SKT, 14 PIN RIGHT ANGLE	14-810-90R	ARIES	2100-03-0072	1
15	SOLDER LUG	11A144	ZIER	2100-04-0025	1
TP1 TP2 TP3 TP4 TP5	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	5
J16	HEADER, 34 PIN	929836-01-17	AP	2100-05-0041	1
Y1	CRYSTAL, 4MHZ	180-502	WVTK	2300-99-0004	1
7	CABLE TIE, 8.00 IN	PLT2M-8.00	PANDT	2800-00-0033	1
11	STANDOFF, SWAGE .125 H, .250 DIA	9531B-0440-3A	AMTOM	2800-03-0004	3

WAVETEK PARTS LIST | TITLE: PCA, MICROPROC BD MODEL 604 | ASSEMBLY NO. 1100-00-1224 | PAGE: 2 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	4-40, .062 MAT'L				
9	SCREW, SELF LOCKING, PAN CROSS RECESS 4-40X1/4	4-40 X 1/4	CMRCL	2800-23-4104	3
J17	JUMPER	461-2871-01-03-10	CAMB	3000-00-0034	1
E1 E2	PINS, JUMPER	450-3704-01-03	CAMB	3000-00-0035	2
K1 K2 K3 K4 K5 K6 K7 K8	RELAY, REED, FORM-A	RA3019-1051	ETROL	4300-00-0007	8
R10 R3	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	2
R13 R7	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	2
R19 R4 R5 R9	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	4
R21	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	1
R20	RES, MF, 1/8W, 1%, 10	RN55D-10R0F	TRW	4701-03-1009	1
R1	RES, MF, 1/8W, 1%, 165	RN55D-1650F	TRW	4701-03-1650	1
R2	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
R6 R8	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	2
RN1 RN2 RN3	RES MODULE, 10K	4310R-101-103	BOURN	4770-00-0008	3
RN4 RN5	RES MODULE	4116R-001-102	BOURN	4770-00-0019	2
RN6 RN7	RES MODULE 303/622	4310R-104-302/622	BOURN	4770-00-0038	2

WAVETEK PARTS LIST | TITLE: PCA, MICROPROC BD MODEL 604 | ASSEMBLY NO. 1100-00-1224 | PAGE: 3 | REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RV1 RV2	VARISTOR	V56ZA8	GE	4799-00-0048	2
CR2	DIODE	1N4002	FAIR	4801-02-0001	1
CR1	DIODE	3N254	MOT	4801-02-0254	1
SW1	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1
4	BUTTON, BONE GRAY	B-305	CRL	5103-04-0009	1
SW2	SWITCH PC	500-105	DUNCN	5199-00-0001	1
T1	TRANSFORMER	DST5-20	SIGNL	5600-00-0029	1
W3	WIRE, HU, 18GA	HH0603-0RN/YELLOW	JUDD	6000-31-8045	1
16	WIRE, HU, 22GA	15U-BROWN	QAVTT	6000-32-2001	1
5	WIRE, HU, 22GA	15U-RED	QAVTT	6000-32-2002	1
17	WIRE, HU, 22GA	15U-ORANGE	QAVTT	6000-32-2003	1
6	SHRINK TUBING, 1/8 IN	FIT-221-1/8	ALPHA	6001-20-2000	1
VR1	IC	LM317T	NSC	7000-03-1700	1
U2	IC	MLM339P	MOT	7000-03-3900	1
U3	IC	MC6803L	MOT	8000-68-0300	1
U6	IC	74LS00	TI	8000-74-0010	1
U9	IC	7438	TI	8000-74-3800	1

WAVETEK PARTS LIST | TITLE: PCA, MICROPROC BD MODEL 604 | ASSEMBLY NO. 1100-00-1224 | PAGE: 4 | REV

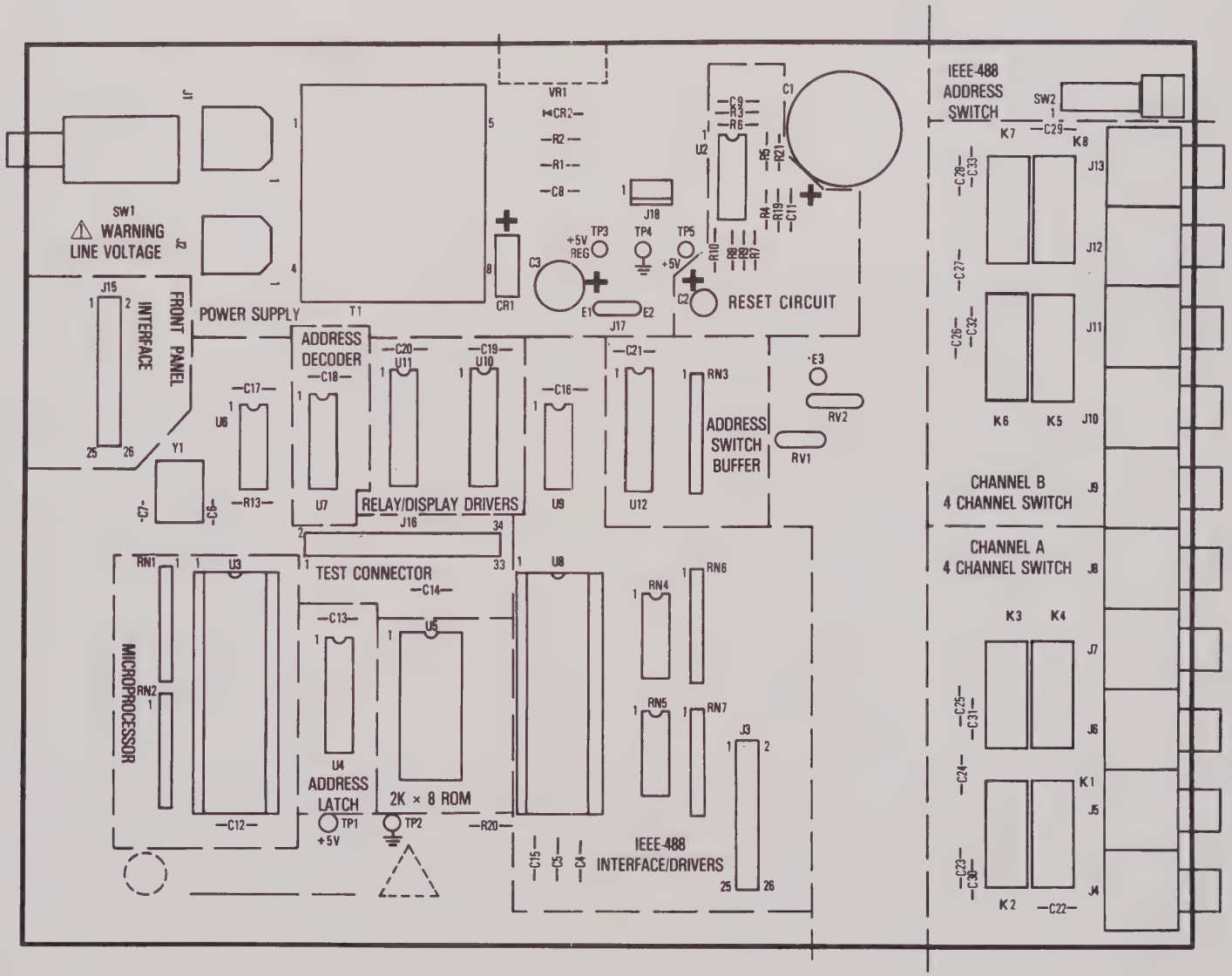
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U8	IC	MC6848BP	MOT	8006-84-8800	1
U7	IC	74LS139	SIG	8007-41-3910	1
U12	IC	74LS244	TI	8007-42-4410	1
U4	IC	74LS373	MOT	8007-43-7310	1
U10 U11	IC	74LS374	TI	8007-43-7410	2
U5	IC, PROGRAMMED REF: 8000-27-1600	8600-00-0273	WVTK	8600-00-0273	1

WAVETEK PARTS LIST | TITLE: PCA, MICROPROC BD MODEL 604 | ASSEMBLY NO. 1100-00-1224 | PAGE: 5 | REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST GPIB/MICROPROC
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 604 / DWG NO 1100-00-1224 / REV
	SCALE		CODE IDENT 23338 / SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: GPIB/MICROPROCESSOR ASSEMBLY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		
	DO NOT SCALE DWG	MODEL NO 604	DWG NO 1100-00-1224 REV
	SCALE	CODE IDENT 23338	SHEET OF

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

MICROPROCESSOR

+5V, RN1 10K, (2D1) (A3) (A5) (D5)

U3 6803: Vss, XTAL1, XTAL2, NMI/, IRQ/, RESET/, Vcc, P20, P21, P22, P23, P24, P10, P11, P12, P13, P14, P15, P16, P17, E, AS, R/W, P30, P31, P32, P33, P34, P35, P36, P37, P40, P41, P42, P43, P44, P45, P46, P47, STBY

(2C1) NMI/, (D5) IRQ/, (2C7) MR/

Y1 4MHZ, C6 27pF S.M., C7 27pF S.M., C12 .1/50V

N.C., (2B6)(2C6) P24, (2A3) P10, (2B3) P11, (2A3) P12, (2B3) P13, (2A3) P14, (2B3) P15, (2A3) P16, (2A3) P17

RN2 10K

AS(2C2), R/W, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, ADR8 (A3)(2C1), ADR9, ADR10, ADR11 (B3)(2C1), ADR12 (A5)(2C1), ADR13 (B8)(2C1), ADR14 (A6)(2C1), ADR15 (A6)(2D1), +5V

ADDRESS LATCH

C13 +5V .1/50V

U4 74LS373: G, OE, D1 Q1 ADR0, D2 Q2 ADR1, D3 Q3 ADR2, D4 Q4 ADR3 (A4), D5 Q5 ADR4 (D5), D6 Q6 ADR5, D7 Q7 ADR6, D8 Q8 ADR7

IEEE-488 INTERFACE / DRIVERS

(D7) ADR0, (D7) ADR1, (D7) ADR2, (D8) IRQ/

U8 68488: Vss, DMAR, DAV/, DAC, RFD, RESET/, Vcc, DMAI, CS/, ASE/, R/W, E, DB0, DB1, DB2, DB3, DB4, DB5, DB6, DB7, IRQ/, RS2, RS1, RS0, IB0/, IB1/, IB2/, IB3/, IB4/, IB5/, IB6/, IB7/, T/R1, T/R2, ATN/, EOI/, TRIG, SRQ/, REN/, IFC/

(A6) GPIB/, (2A7) ASE/, (D7) R/W, (D7) E, AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7, (D7), N.C., (2C7) MR/

C15 .1/50V, C4 .01/50V, C5 .01/50V

RN4 1K, RN5 1K

RN6 6.2K(8) 3K(8), RN7 6.2K(8) 3K(8)

IEEE-488 CONN J3-: DIO1/, DIO2/, DIO3/, DIO4/, DIO5/, DIO6/, DIO7/, DIO8/, N.C., ATN/, EOI/, SRQ/, REN/, IFC/, DAV/, DAC, RFD

ADDRESS DECODER

C16 .1/50V, C17 .1/50V, C18 .1/50V

7438: U9-A, U9-B, U9-C, U9-D

1/4 74LS00: U6-A, U6-B, U6-C, U6-D

(C7) ADR13, TEST/ (2B1), R13 10K

U7A, U7B 1/2 74LS139: (C7) ADR14, ADR15, (D6) E, ADR12 (C7), N.C., GPIB/(D5), ROM/(A3), R2/(2B6), R1/(2C6)

2K x 8 ROM

TP1, TP2, C14 .1/50V, U5: ADR7, ADR6, ADR5, ADR4, ADR3, ADR2, ADR1, ADR0, AD7, AD6, AD5, AD4, AD3, (C6), (D7), ADR8(C7), ADR9(C7), ADR10(C7), ROM/(A6), (C7)

R20 10, ADR11(C6)

P/N 8600-00-0273

1. ALL RESISTORS ARE 1/8 W, 1% IN OHMS.
2. ALL CAPACITORS ARE IN MICROFARADS.

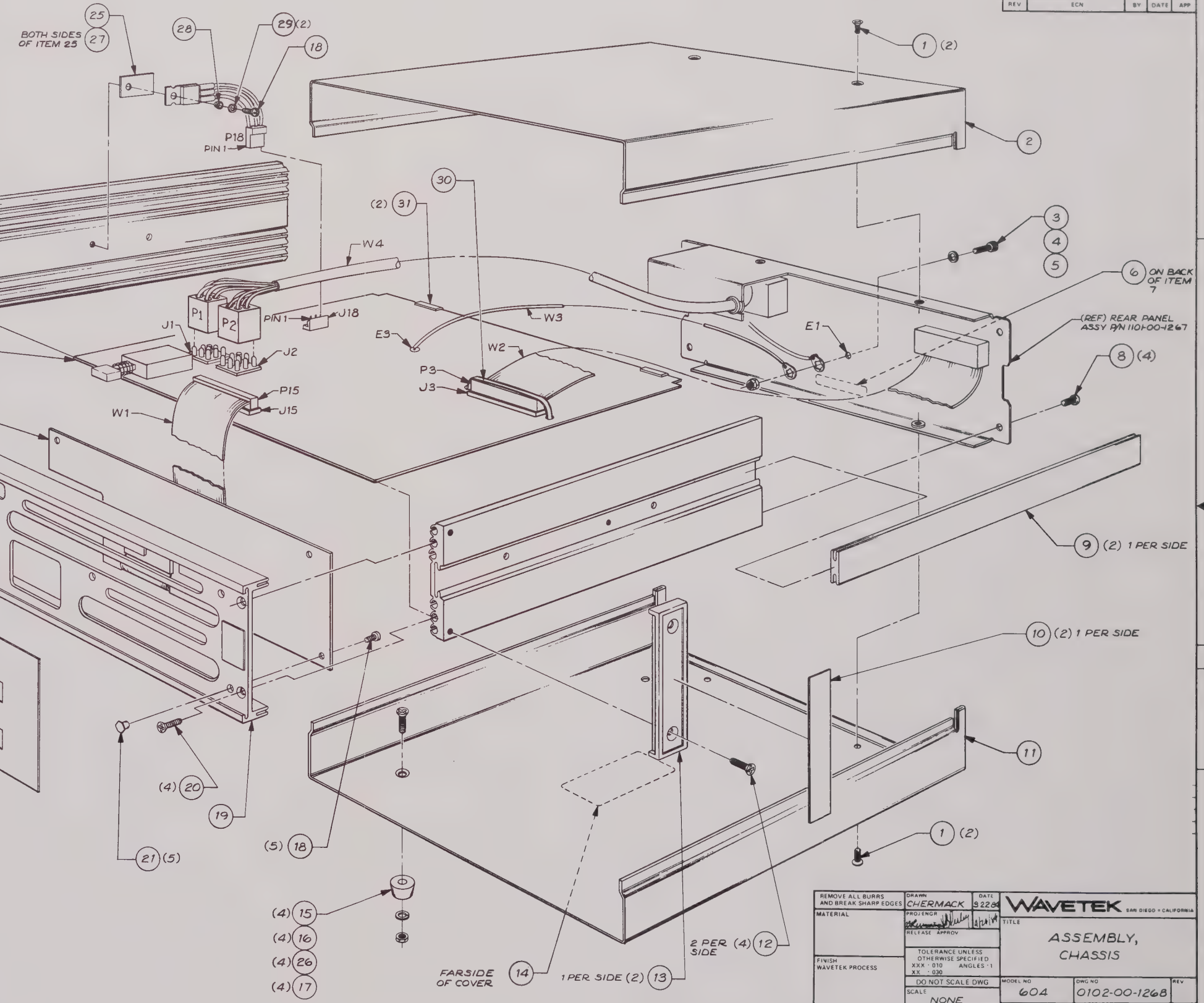
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 3-1880	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR Dan Cummings	4/24/81	TITLE: SCHEMATIC, GPIB/MICROPROC BD
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 604
	SCALE		DWG NO 0103-00-1224 REV
			CODE IDENT 23338 SHEET 1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3884

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 9 22 89	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: ASSEMBLY, CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 604	DWG NO 0102-00-1268 REV
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS ACCUPRESS REORDER NO A27085

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, CHASSIS	0102-00-1268	WVTK	0102-00-1268	1
6	SERIAL TAG MODEL 602	1400-01-6950	WVTK	1400-01-6950	1
14	LABEL,FCC COMPLIANCE	1400-01-7160	WVTK	1400-01-7160	1
11	COVER, BOTTOM	1400-01-7782	WVTK	1400-01-7782	1
2	COVER, TOP	1400-01-7792	WVTK	1400-01-7792	1
22	FRONT PANEL FACEPLATE	1400-01-7800	WVTK	1400-01-7800	1
19	FRONT, SUBPANEL	1400-01-7812	WVTK	1400-01-7812	1
24	SIDE PLATE	1400-01-7830	WVTK	1400-01-7830	2
13	FRONT VERTICAL TRIM CAP	1400-01-7841	WVTK	1400-01-7841	2
10	DECAL, DRESS	1400-01-7920	WVTK	1400-01-7920	2
9	INSERT, SIDE PANEL REF: 3200-06-0048	1400-01-7931	WVTK	1400-01-7931	2
NONE	EDGE TRIM, PCB REF: 3200-06-0053	1400-01-7951	WVTK	1400-01-7951	2
23	TAPE,MASK,3/4" DS	MASKING TAPE 3/4 DS	PRMCL	1600-02-0007	2
27	THERMAL COMP	120-2	WAKE	1600-03-0001	1
31	TIE STRAP	SST-1.5M	PANDT	2800-00-0003	1

WAVETEK PARTS LIST	TITLE ASSY, CHASSIS MODEL 604	ASSEMBLY NO. 1101-00-1268 PAGE: 1	REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
21	STANDOFF, PRESS .187, .100 MAT'L 4-40, .165DIA	SO-440-6	PEM	2800-06-0016	5
15	FOOT,RUBBER	2197W	ROYAL	2800-08-0013	4
28	WASHER	B51547F013	MOT	2800-11-0015	1
17	SCREW, HEX NUT, CAD PLATE 6-32	MS35649-264	COML	2800-14-6100	4
5	NUT, FLEXLOCK, CAD I 6-32	6-32 NUT F.L.	CMRCL	2800-15-6100	1
3	SCREW, SOC CAP, CAD I 6-32X3/8	6-32 X 3/8 S.C.	CMRCL	2800-18-6106	1
12	SCREW, F.H. CAD I, CROSS RECESS, 8-32 X 1/2	8-32 X 1/2 F.H.	CMRCL	2800-19-8108	4
8	SCREW, SELF TAPPING TYPE B, PAN CROSS RECESS, 8X1/2	8-18 X 1/2	CMRCL	2800-22-8208	4
20	SCREW,SELF TAPPING TYPE B,FLAT HD 82DEG 8-16X1/2CROSS RECESS	8-16X1/2 F.H.	CMRCL	2800-22-8908	4
18	SCREW, SELF LOCKING, PAN CROSS RECESS 4-40X1/4	4-40 X 1/4	CMRCL	2800-23-4104	6
29	WASHER, FLAT,	NAS620-4	CMRCL	2800-26-4001	2

WAVETEK PARTS LIST	TITLE ASSY, CHASSIS MODEL 604	ASSEMBLY NO. 1101-00-1268 PAGE: 2	REV

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	4(.209 O.D.)				
4	WASHER, FLAT, #6 BIN 495	#6FLAT WASHER	CMRCL	2800-26-6001	1
16	SCREW, PAN, CAD PLATE, 6-32X1/2	6-32 X 1/2	CMRCL	2800-38-6108	4
26	WASHER, SPLIT LOCK, 6	#6SRLW	CMRCL	2800-42-6000	4
1	SCREW,6-32X3/8 FH MS 100DEG,PHLPS BLK	2800-43-6106	WVTK	2800-43-6106	4
25	INSULATOR,MICA	64-21-023-106	ASHVL	3100-00-0006	1

WAVETEK PARTS LIST	TITLE ASSY, CHASSIS MODEL 604	ASSEMBLY NO. 1101-00-1268 PAGE: 3	REV

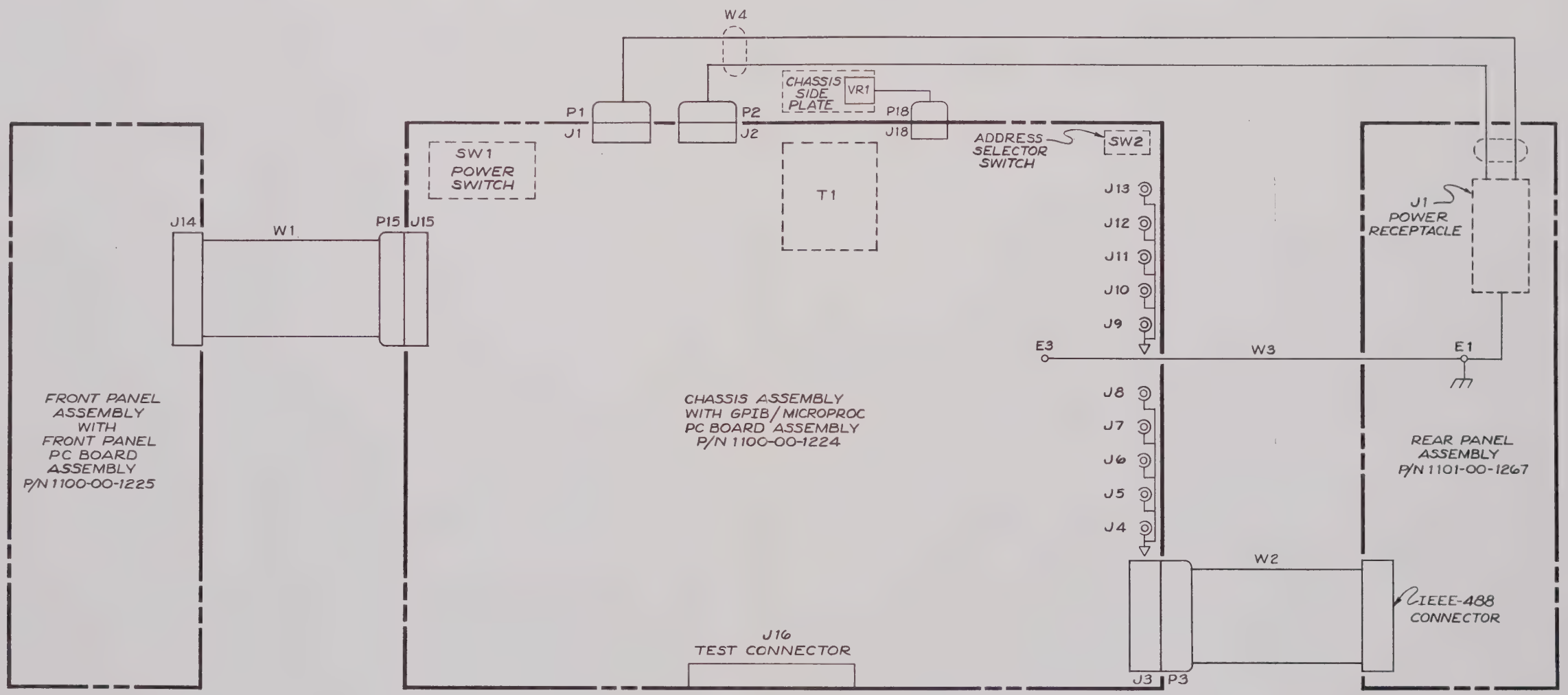
NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		MODEL NO 604 / DWG NO. 1101-00-1268 / REV
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 1
	SCALE		

BISHOP GRAPHICS ACCUPRESS REORDER NO. A37086

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP



NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 3-26-84	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR Van Cumming	4/11/84	TITLE SCHEMATIC, INSTRUMENT
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 64	DWG NO 0004-00-0253 REV
	SCALE N/A	CAGE CODE 23338	SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, MODEL 604	0002.00.0253	WVTK	0002-00-0253	1
NONE	INSTRUMENT SCHEMATIC MODEL 604	0004-00-0253	WVTK	0004-00-0253	1
NONE	SPECIFICATIONS	0007-00-0253	WVTK	0007-00-0253	1
NONE	INSTRUMENT OVERALL DIMENSION	0009-00-0253	WVTK	0009-00-0253	1
NONE	PCA, MICROPROC BD MODEL 604	604-1224	WVTK	1100-00-1224	1
NONE	PCA, FRONT PANEL MODEL 604	604-1225	WVTK	1100-00-1225	1
NONE	ASSY, REAR PANEL MODEL 604	604-1267	WVTK	1101-00-1267	1
NONE	ASSY, CHASSIS MODEL 604	604-1268	WVTK	1101-00-1268	1

WAVETEK PARTS LIST	TITLE MODEL 604	ASSEMBLY NO. 1000-00-0253 PAGE: 1	REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE PARTS LIST MODEL 604
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO.	DWG NO. 1000-00-0253 REV
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS ACCUPRESS REORDER NO. A27008

SECTION 6
PARTS AND SCHEMATICS

6.1 DRAWINGS

The following assembly drawings (with parts lists) and schematics are in the arrangement shown below.

6.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

6.3 ORDERING PARTS

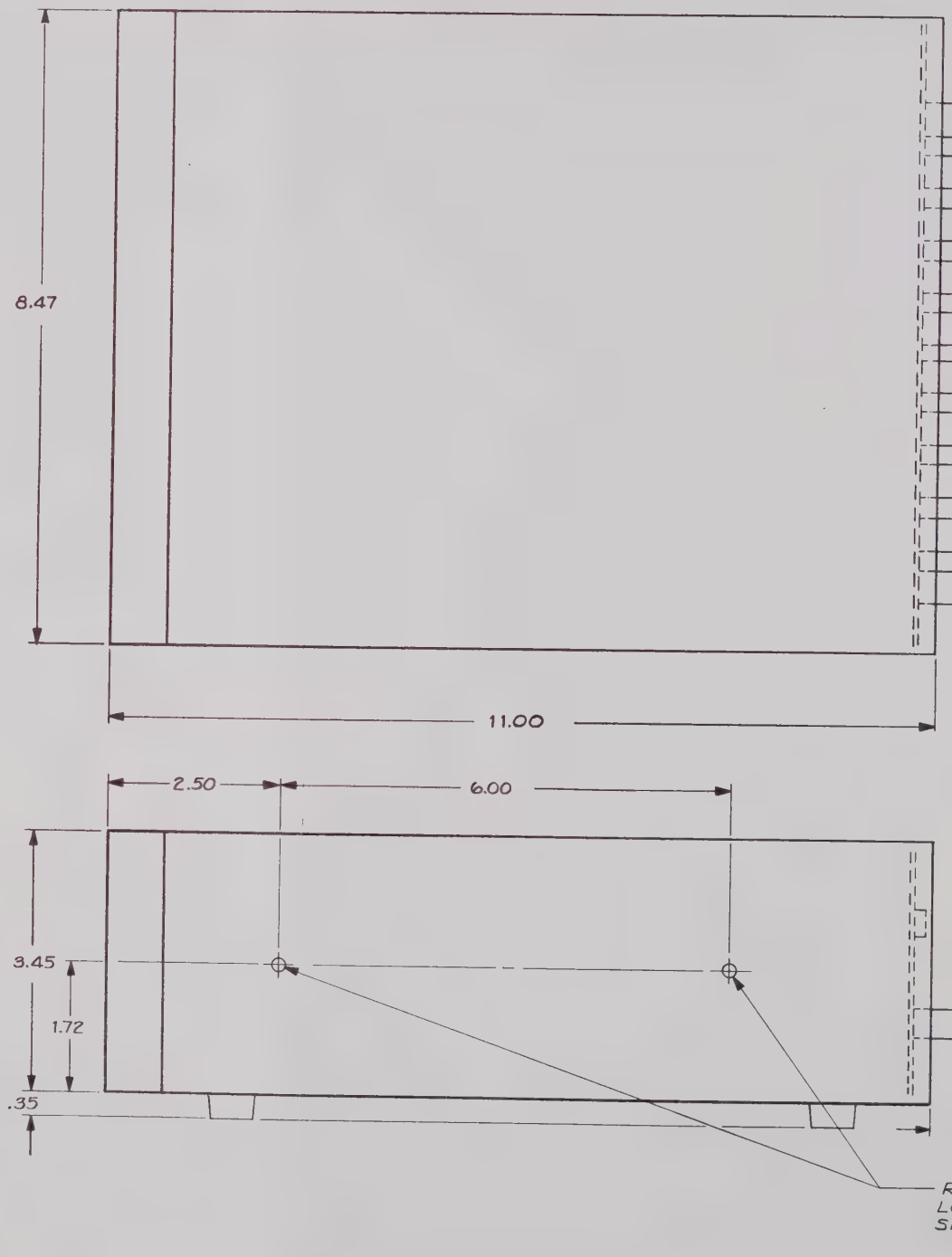
When ordering spare parts, please specify part number, circuit reference board, serial number of unit, and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

DRAWING	DRAWING NUMBER
Instrument Overall Dimensions	0009-00-0253
Instrument Schematic	0004-00-0253
Model 604 Parts List	1000-00-0253
Chassis Assembly	0102-00-1268
Chassis Parts List	1101-00-1268
GPIB/Microprocessor Assembly	1100-00-1224
GPIB/Microprocessor Schematic	0103-00-1224
GPIB/Microprocessor Parts List	1100-00-1224
Front Panel Assembly	1100-00-1225
Front Panel Schematic	0103-00-1225
Front Panel Parts List	1100-00-1225
Rear Panel Assembly	0102-00-1267
Rear Panel Parts List	1101-00-1267

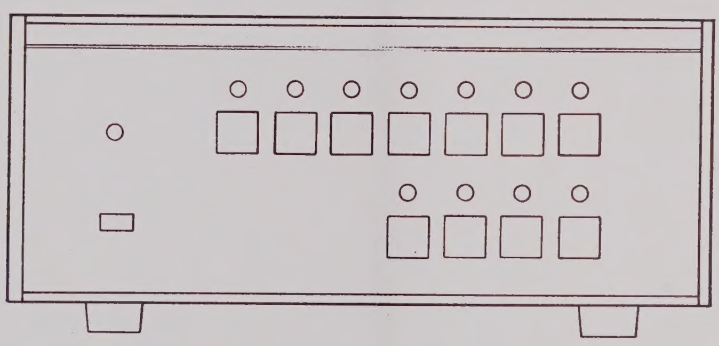
THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



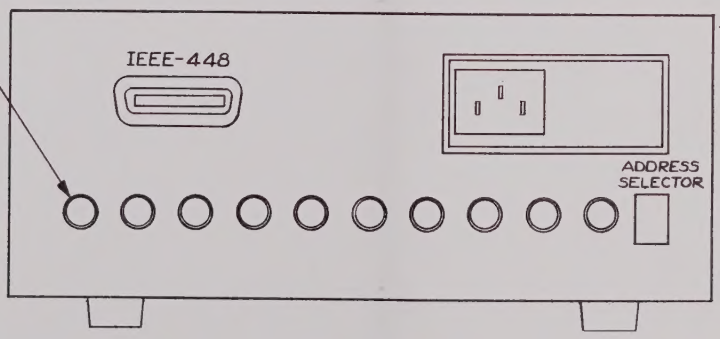
NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS ACCUPRESS
REORDER NO. A27086

REV	ECN	BY	DATE	APP



REAR PANEL
BNC LOCATION



MOUNT HOLE
ONS (TYP BOTH

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 3/28/84	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: INSTRUMENT OVERALL DIMENSIONS (604)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX		MODEL NO. 604 / DWG NO. 0009-00-0253 / REV
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 1
	SCALE 1/1		

MP MASTER
MA35668